MS-7154 *Version 0A*

INTEL (R) Brookdale Chipset
Willamette/Northwood 478pin mPGA-B Processor Schematics

CPU:

Willamette/Northwood mPGA-478B Processor

System Brookdale Chipset:

INTEL GMCH (North Bridge) + INTEL ICH4 (South Bridge)

On Board Chipset:

BIOS -- FWH

AC'97 Codec -- ALC655

LPC Super I/O -- W83627THF

Clock Generation -- ICS952611BF

LAN -- RTL8100C

Expansion Slots:
PCI2.2 SLOT * 5

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Title: Cover Sheet

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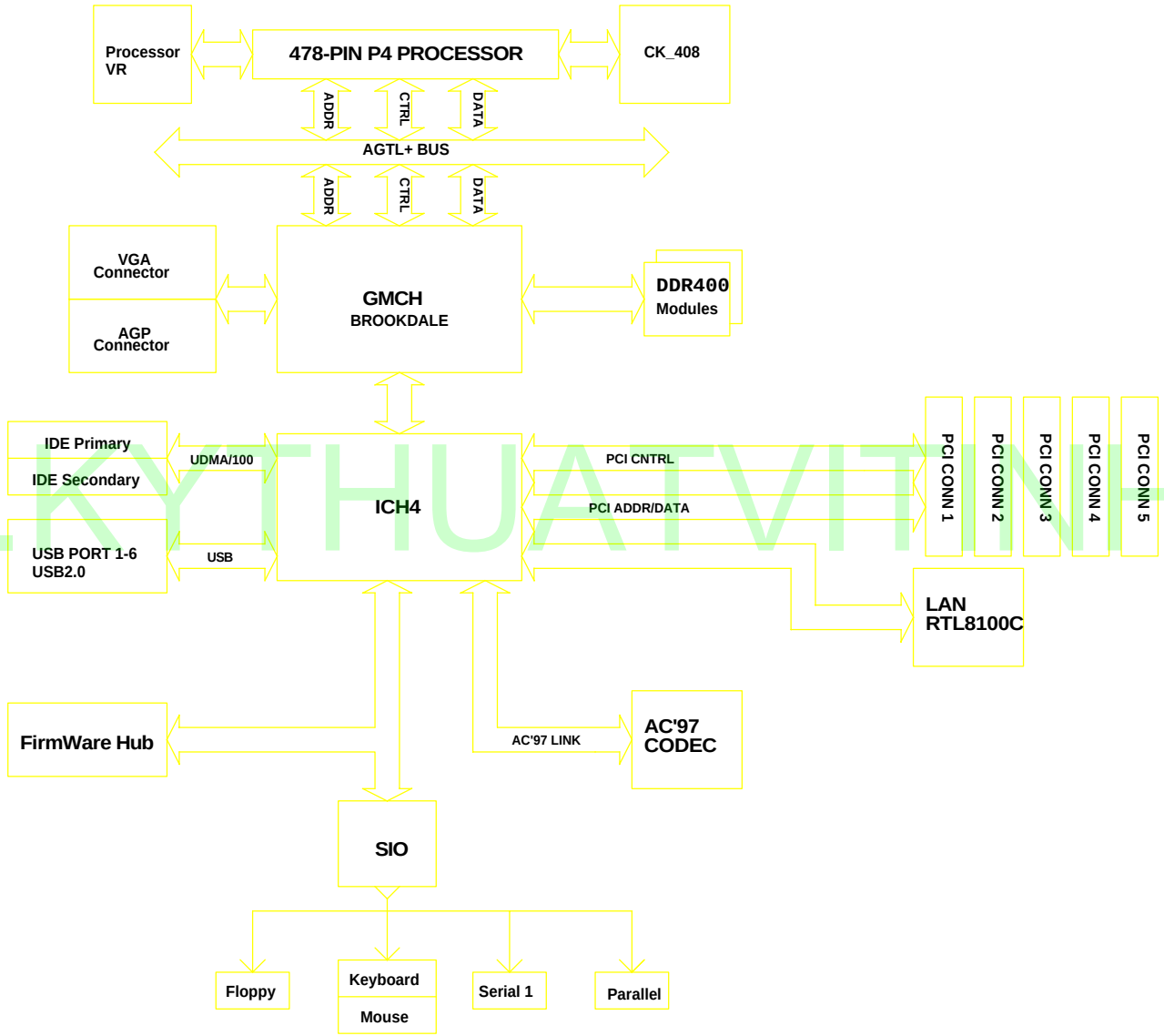
DDR333

BLOCK DIAGRAM



MSI	MICRO-STAR INT'L CO.,LTD.	
Title	Block Diagram	
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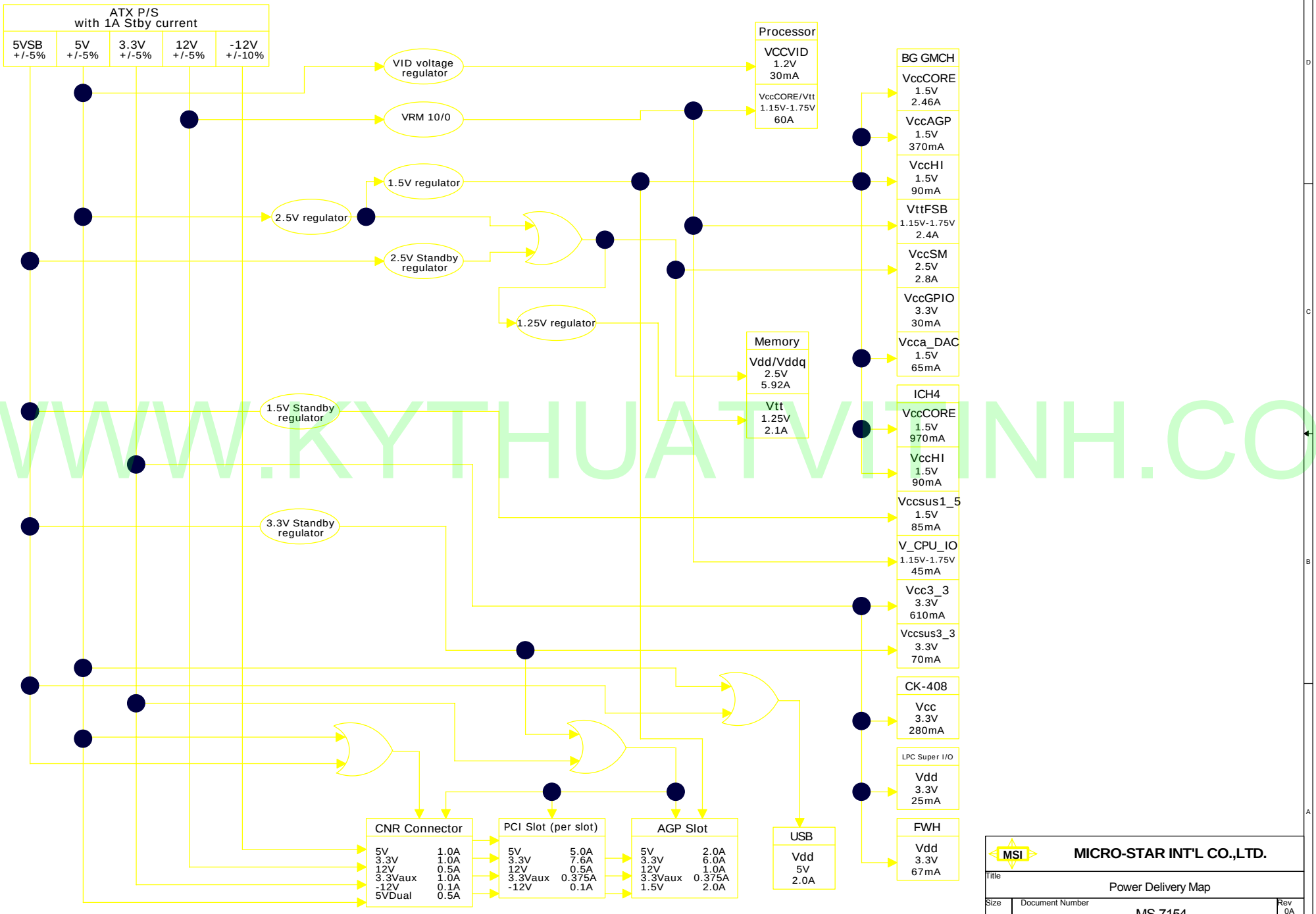
Power Delivery Map



MSI **MICRO-STAR INT'L CO.,LTD.**

Title	Power Delivery Map
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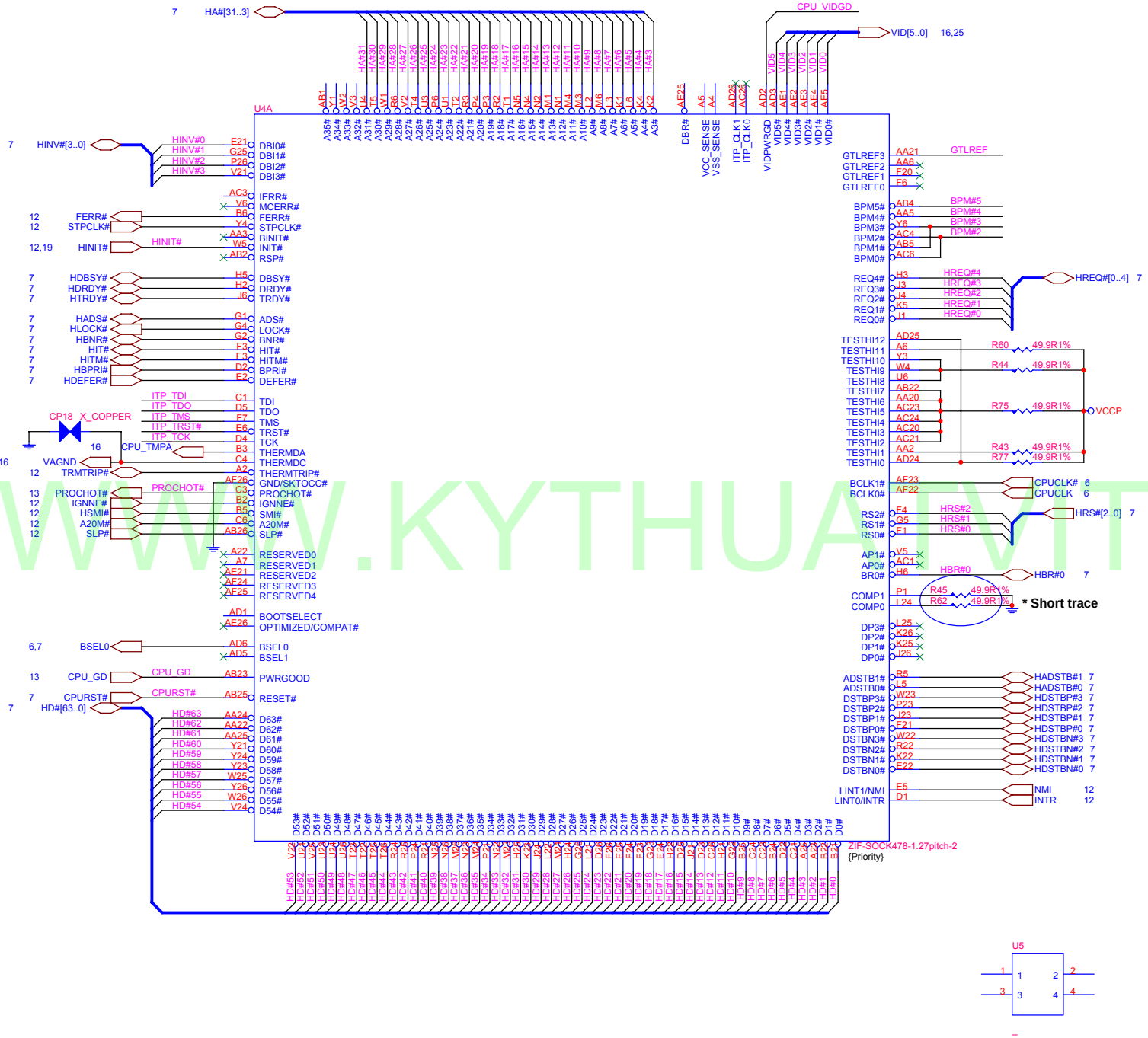
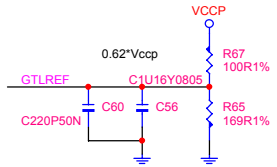
CPU SIGNAL BLOCK

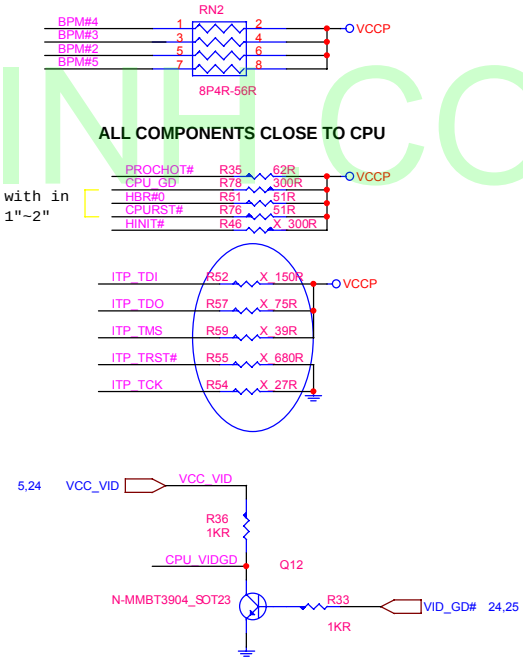


CPU GTL REFERNCE VOLTAGE BLOCK



Every pin put one 220pF cap near it.
Trace Width 7mils,
Space 10mils.
Keep the voltage divider within 1.5" of the GETREF pin.

CPU STRAPPING RESISTORS



MSI	MICRO-STAR INT'L CO.,LTD.	
Title	mPGA478-B INTEL CPU SOCKET Part1	
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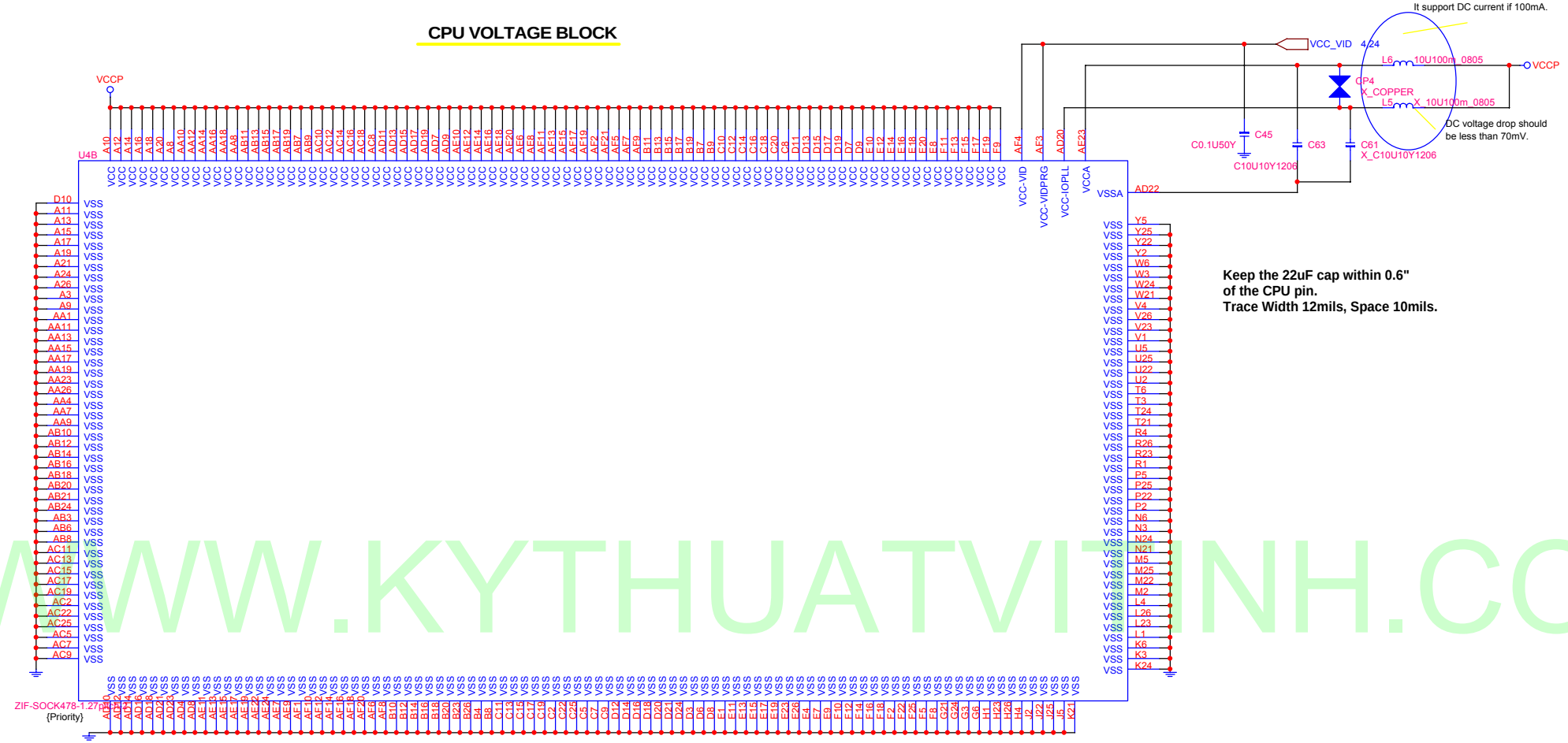
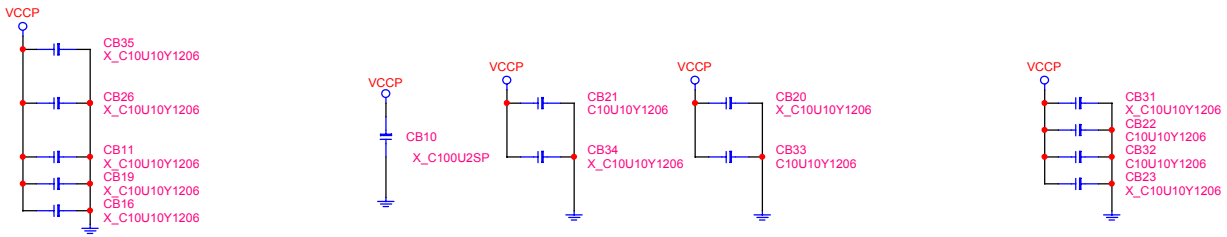
CPU VOLTAGE BLOCK



CPU DECOUPLING CAPACITORS



Place 14 pcs 1206 size cap north side of processor

PLACE CAPS WITHIN CPU CAVITY

MSI	MICRO-STAR INT'L CO.,LTD.	
Title	mPGA478-B INTEL CPU Part2	
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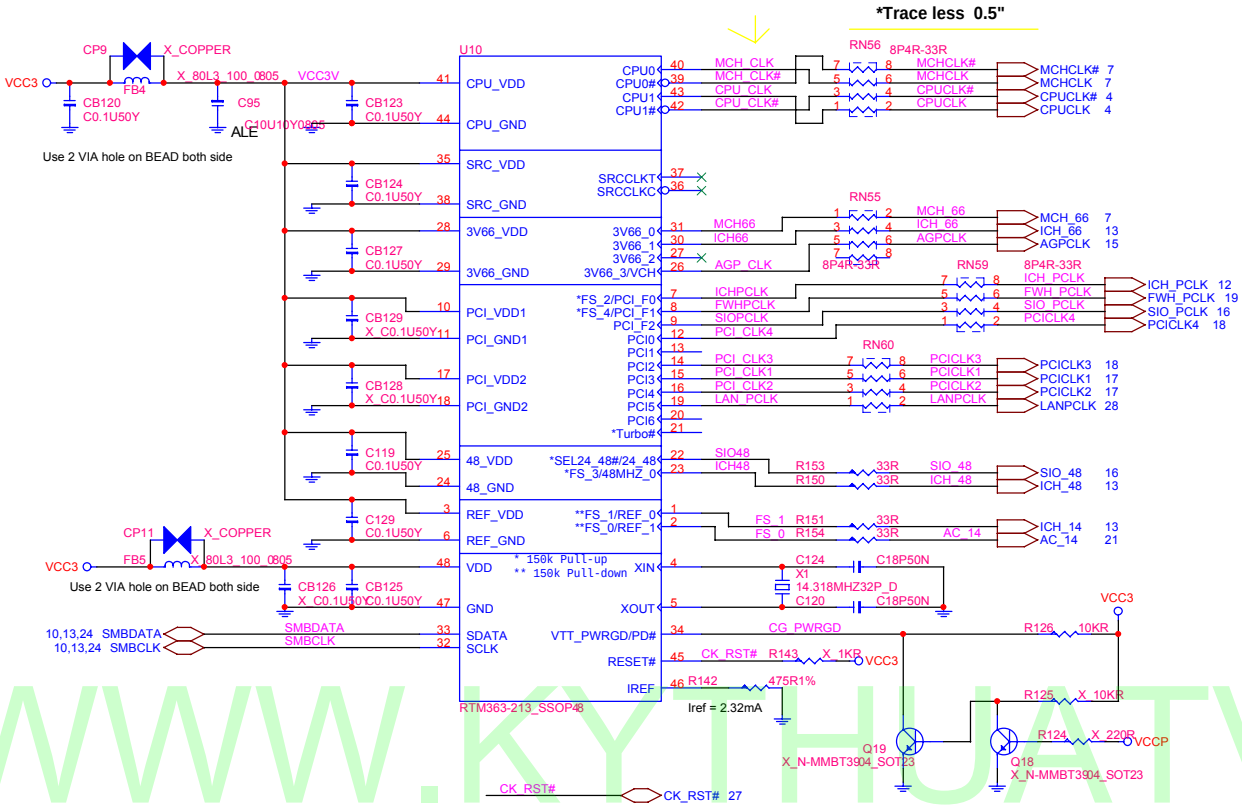
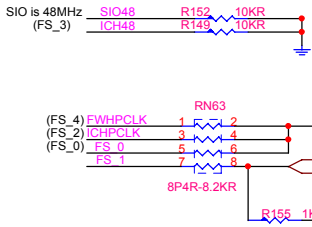


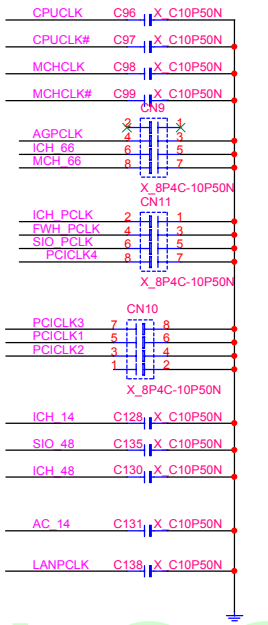
Shut Source Termination Resistors

Trace less 0.2"
49.9ohm for 50ohm M/B impedance

FS_4	FS_3	FS_2	FS_1	FS_0	CPU
0	0	0	0	0	100
0	0	0	0	1	200
0	0	0	1	0	133.3
0	0	0	1	1	166.7



Pull-Down Capacitors

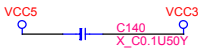


EMC HF filter capacitors, located close to PLL

Ioh=6*Iref
Voh=0.71V

used only for EMI issue

Trace less 0.2"



MSI MICRO-STAR INT'L CO.,LTD.

Title: Clock ICS952611

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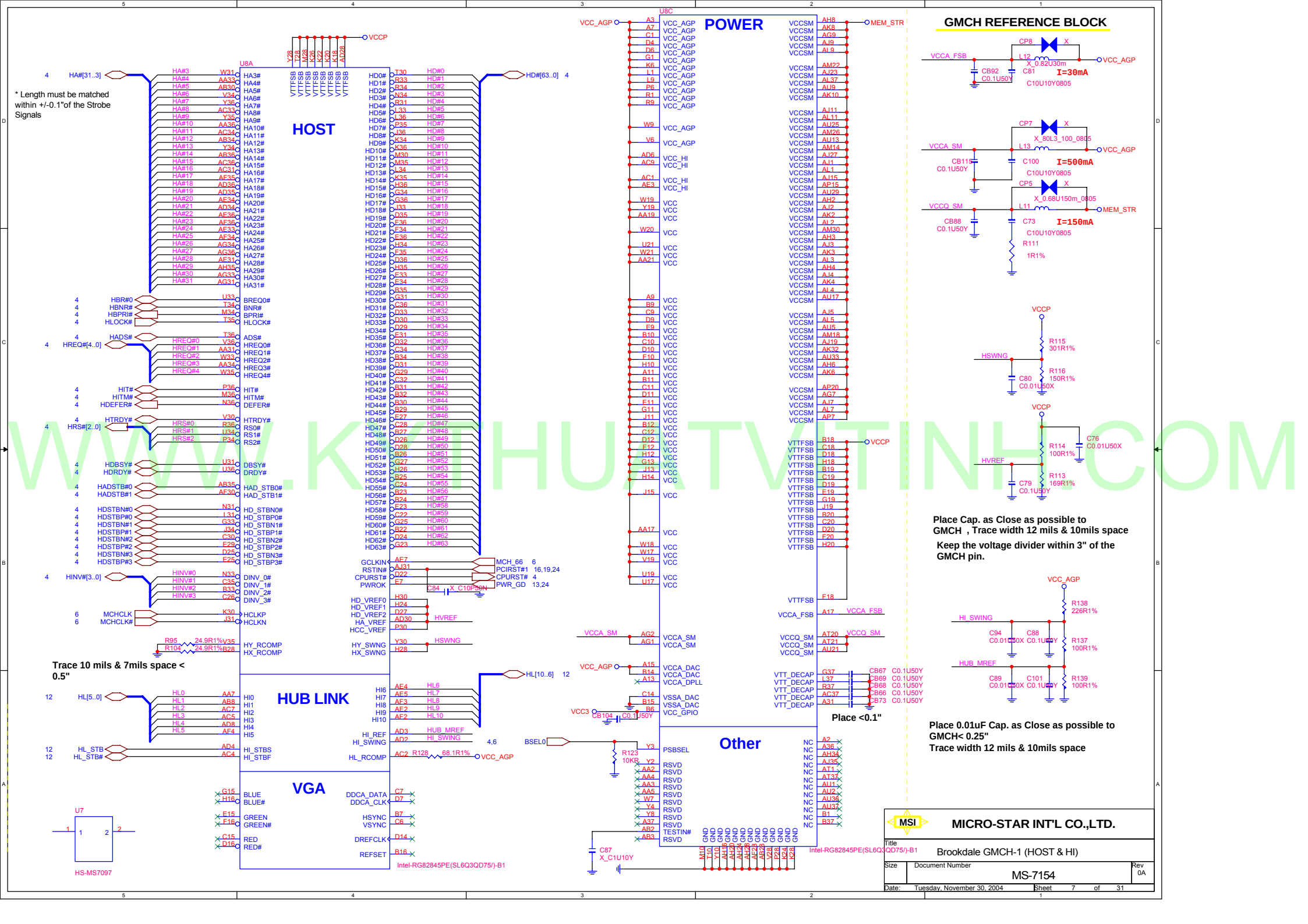

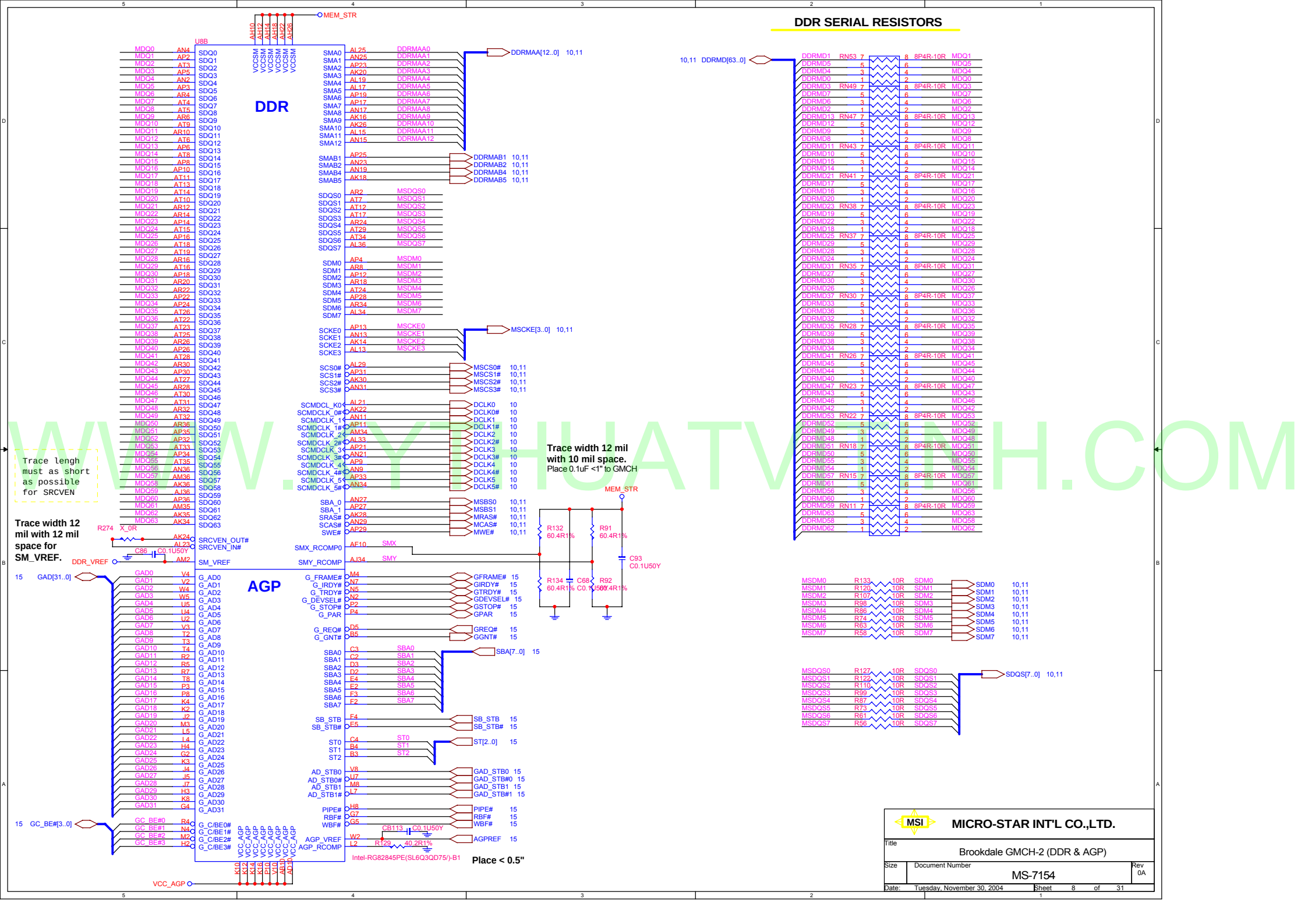
DDR SERIAL RESISTORS
DDR
AGP
U8B
MEM_STR
DDRMAA[12..0] 10,11
DDRMAB1 10,11
DDRMAB2 10,11
DDRMAB4 10,11
DDRMAB5 10,11
MSCKE[3..0] 10,11
MSCS0# 10,11
MSCS1# 10,11
MSCS2# 10,11
MSCS3# 10,11
DCLK0 10
DCLK0# 10
DCLK1 10
DCLK1# 10
DCLK2 10
DCLK2# 10
DCLK3 10
DCLK3# 10
DCLK4 10
DCLK4# 10
DCLK5 10
DCLK5# 10
MSBS0 10,11
MSBS1 10,11
MRAS# 10,11
MCAS# 10,11
MWE# 10,11
SBA[7..0] 15
ST[2..0] 15
GAD_STB0 15
GAD_STB#0 15
GAD_STB1 15
GAD_STB#1 15
PIPE# 15
RBF# 15
WBF# 15
SB_STB 15
SB_STB# 15
GFRAME# 15
GIRDY# 15
GTRDY# 15
GDEVSEL# 15
GSTOP# 15
GPAR 15
GREQ# 15
GGNT# 15
AGPREF 15
10,11 DDRMD[63..0]
SDQS[7..0] 10,11
15 GAD[31..0]
15 GC_BE#[3..0]
Trace lengh must as short as possible for SRCVEN
Trace width 12 mil with 12 mil space for SM_VREF.
Trace width 12 mil with 10 mil space.
Place 0.1uF <1" to GMCH
Place < 0.5"
Intel-RG82845PE(SL6Q3QD75/)-B1
MICRO-STAR INT'L CO.,LTD.
Brookdale GMCH-2 (DDR & AGP)
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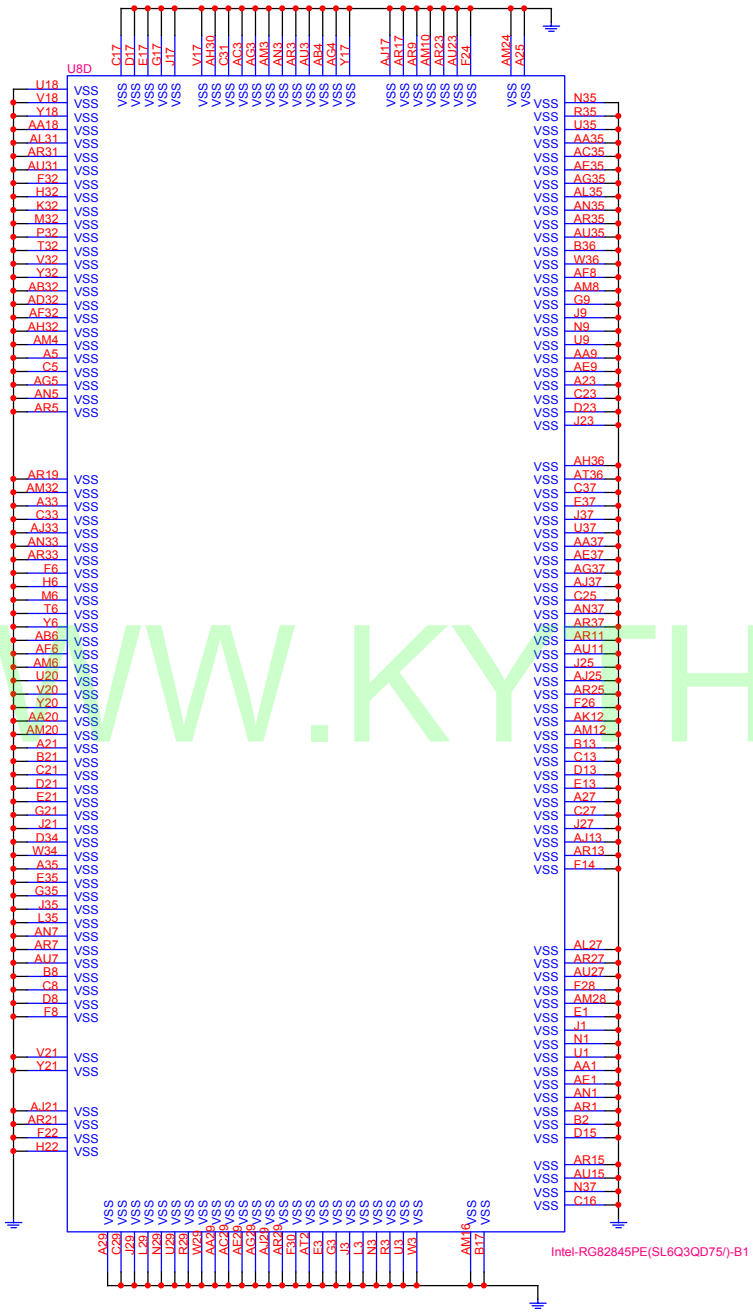
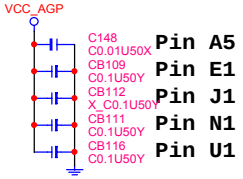
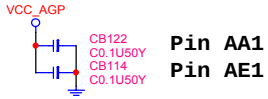


GMCH DECOUPLING CAPACITOR



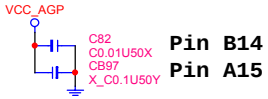
Pin A5
Pin E1
Pin J1
Pin N1
Pin U1

Place decoupling cap close to GMCH AGP Interface < 0.1"



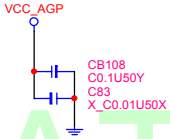
Pin AA1
Pin AE1

Place decoupling cap close to GMCH Hub-Link Interface< 0.1"

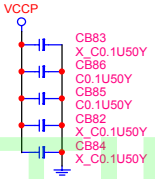


Pin B14
Pin A15

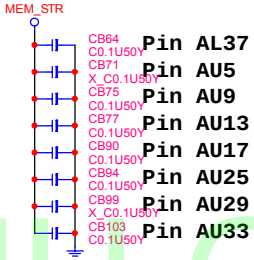
Place decoupling cap close to GMCH DAC Interface< 0.1"



Place decoupling cap close to GMCH Core Logic Interface < 0.1"

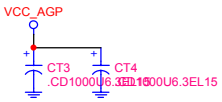


Place decoupling cap close to GMCH CPU Interface < 250mil in the Vtt corridor

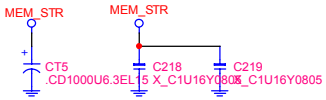


Pin AL37
Pin AU5
Pin AU9
Pin AU13
Pin AU17
Pin AU25
Pin AU29
Pin AU33

Place decoupling cap close to GMCH Memory Interface < 0.1", with 18 mil trach width



Place Bulk cap for Core Logic, AGP & Hub Link Interface



Place Bulk cap between GMCH & DIMM slot

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Title	Brookdale GMCH(VSS)		
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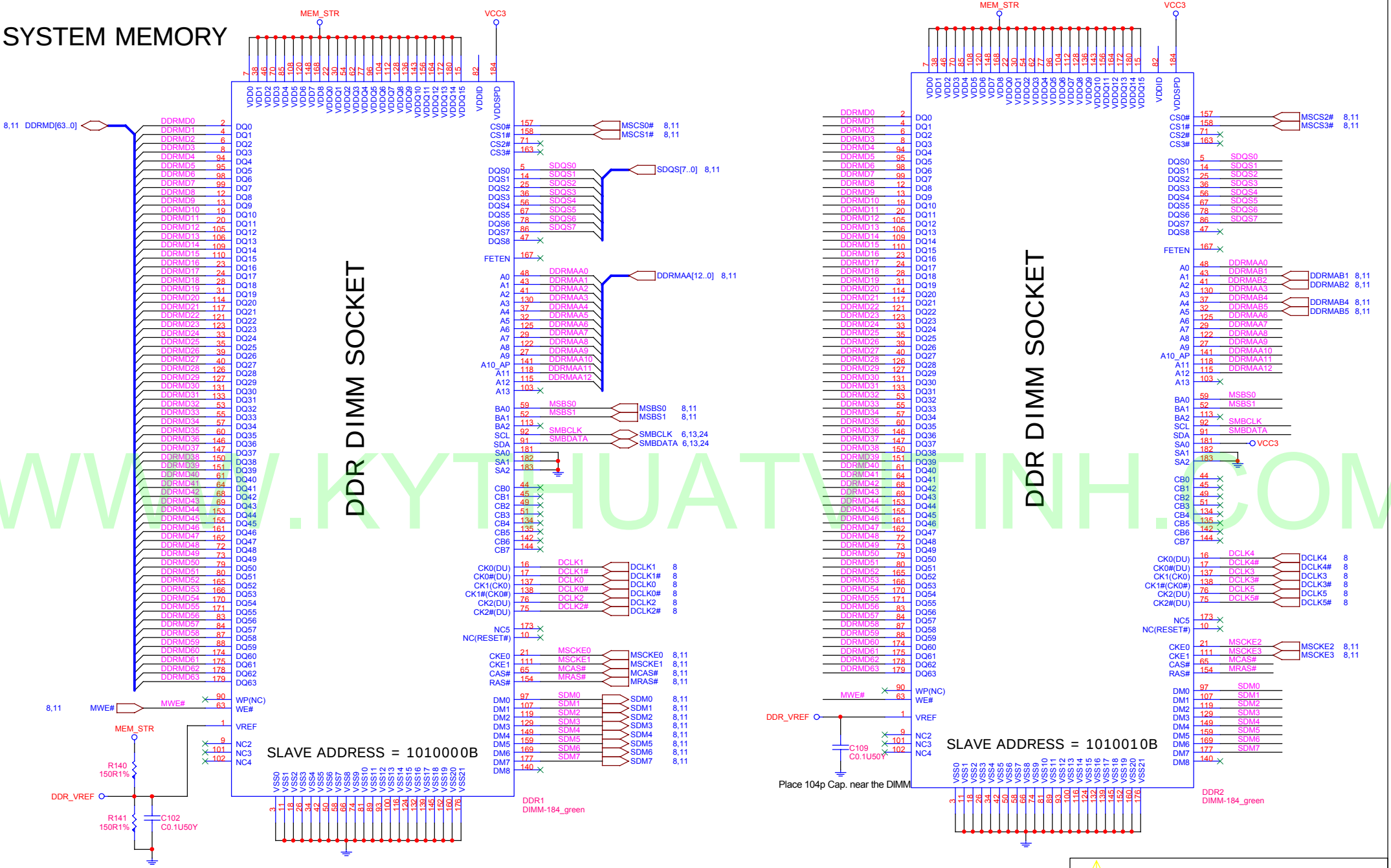
SYSTEM MEMORY



Keep the voltage divider within 1" of DIMM1.
Trace width 12 mil with 12 mil space.
Place 104p Cap. near the DIMM

MSI **MICRO-STAR INT'L CO.,LTD.**

Title	DDR DIMM1&2	
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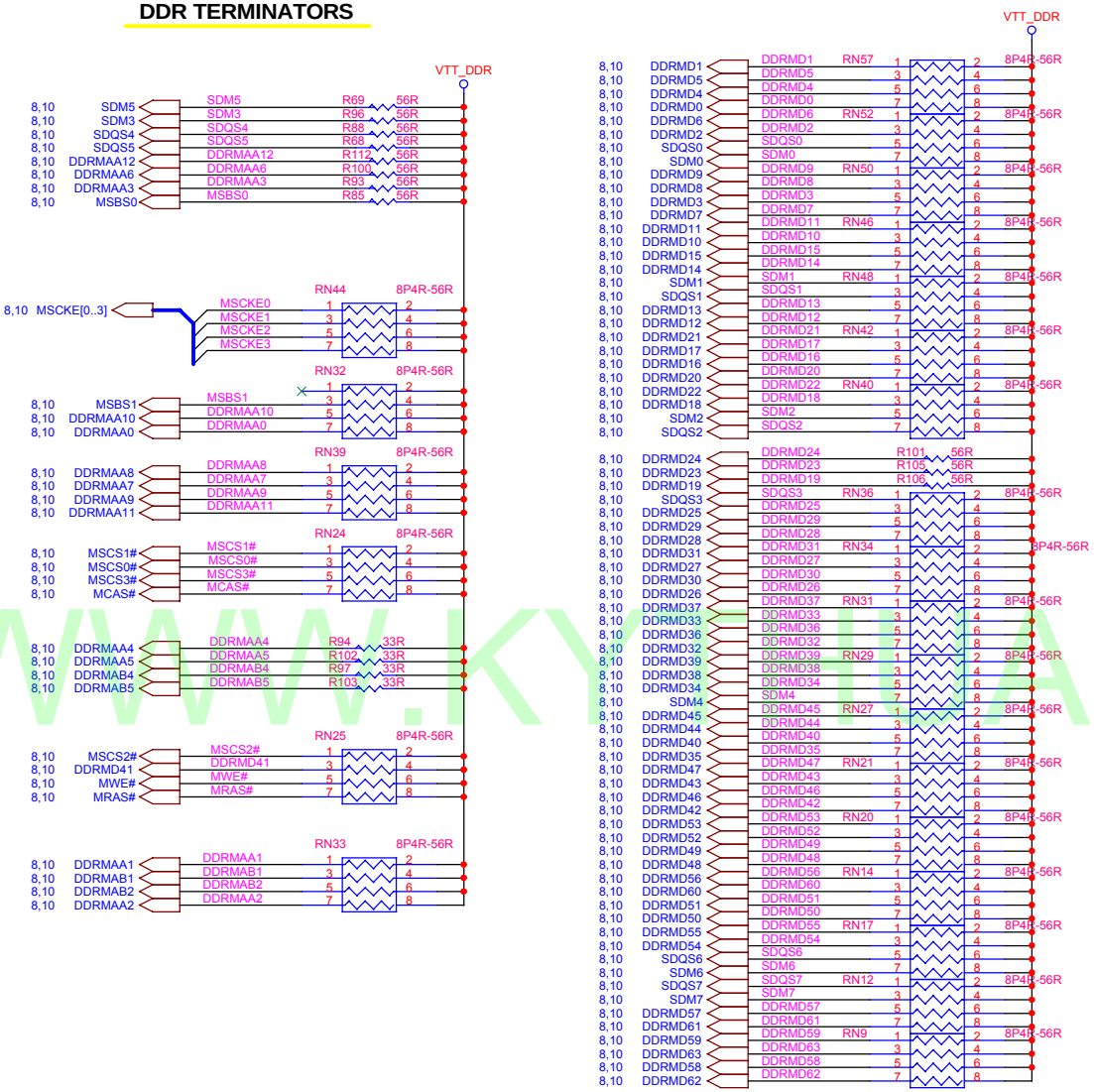
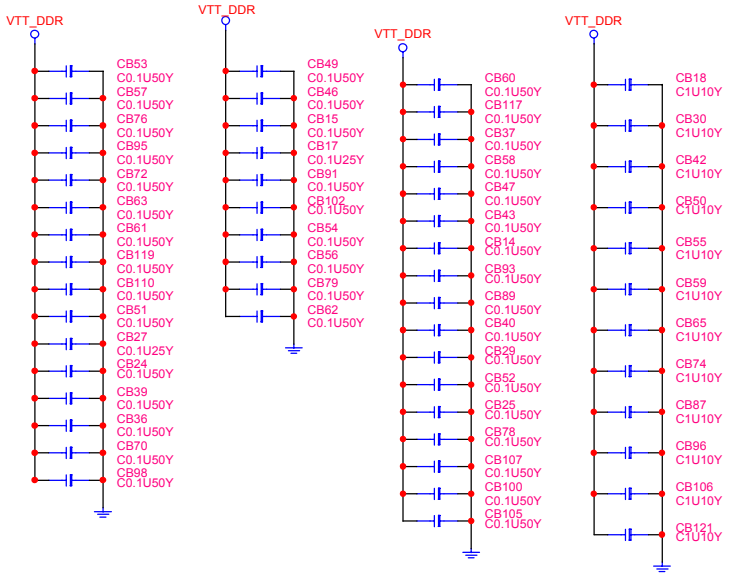
DDR TERMINATORS

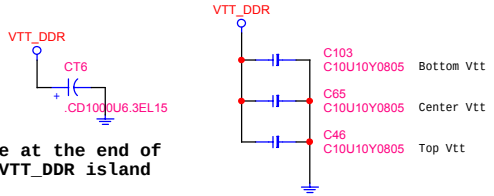


DDR Decouping Caps



Total 110 signal, need 55 pcs decoupling.

Place for VTT_DDR island



Place at the end of the VTT_DDR island

MSI **MICRO-STAR INT'L CO.,LTD.**

Title	DDR Terminator Resistor	
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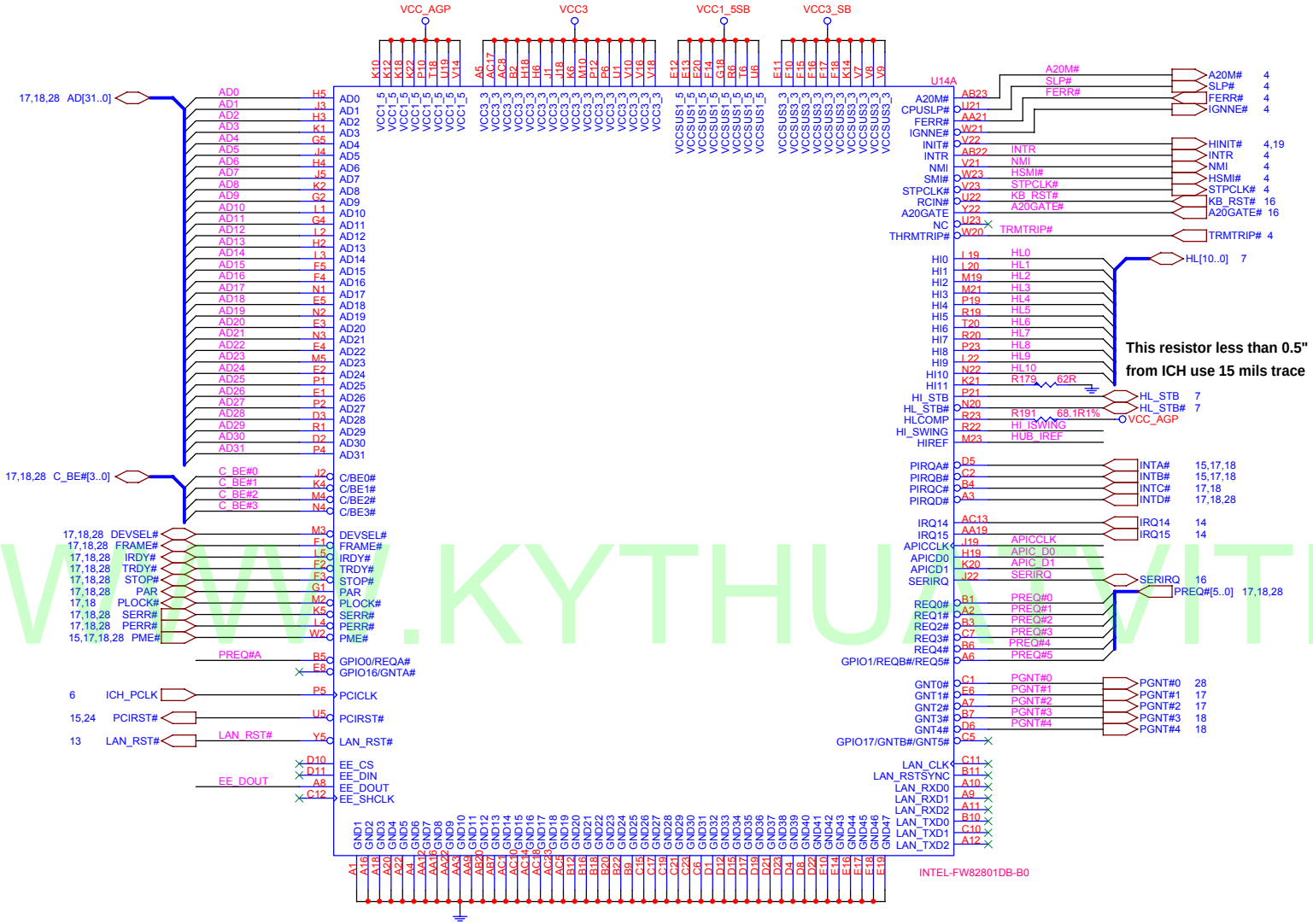
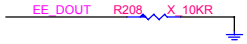
ICH4 PCI / HUB LINK / CPU / LAN / INTERRUPT SIGNALS

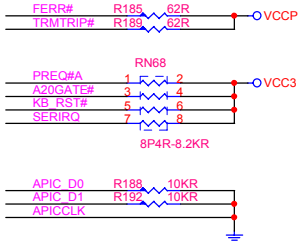


ICH4 STRAPPING RESISTORS

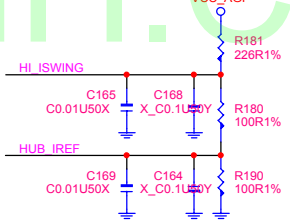


Reserved pull-down resistor for ICH4 reserved function straps.

ICH4 PULL-UP/DOWN RESISTORS



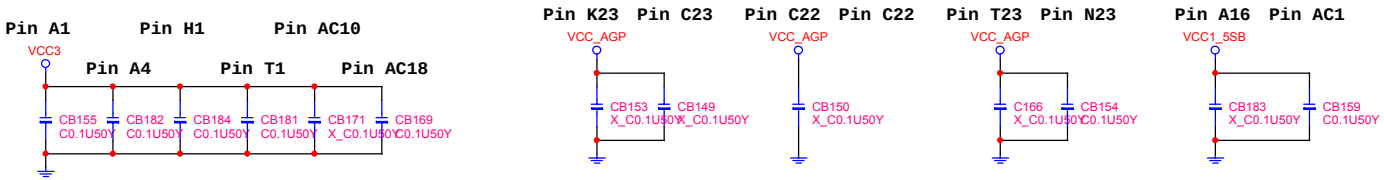
ICH4 REFERENCE VOLTAGE



Place Cap. as Close as possible to ICH4 < 0.25"
Trace width use 12 mils and 10mils space

ICH4 DECOUPLING CAPACITORS

Place one 0.1u close to ICH4 <100 mil



MSI	MICRO-STAR INT'L CO.,LTD.	
Title	ICH4 PCI & HI & LAN	
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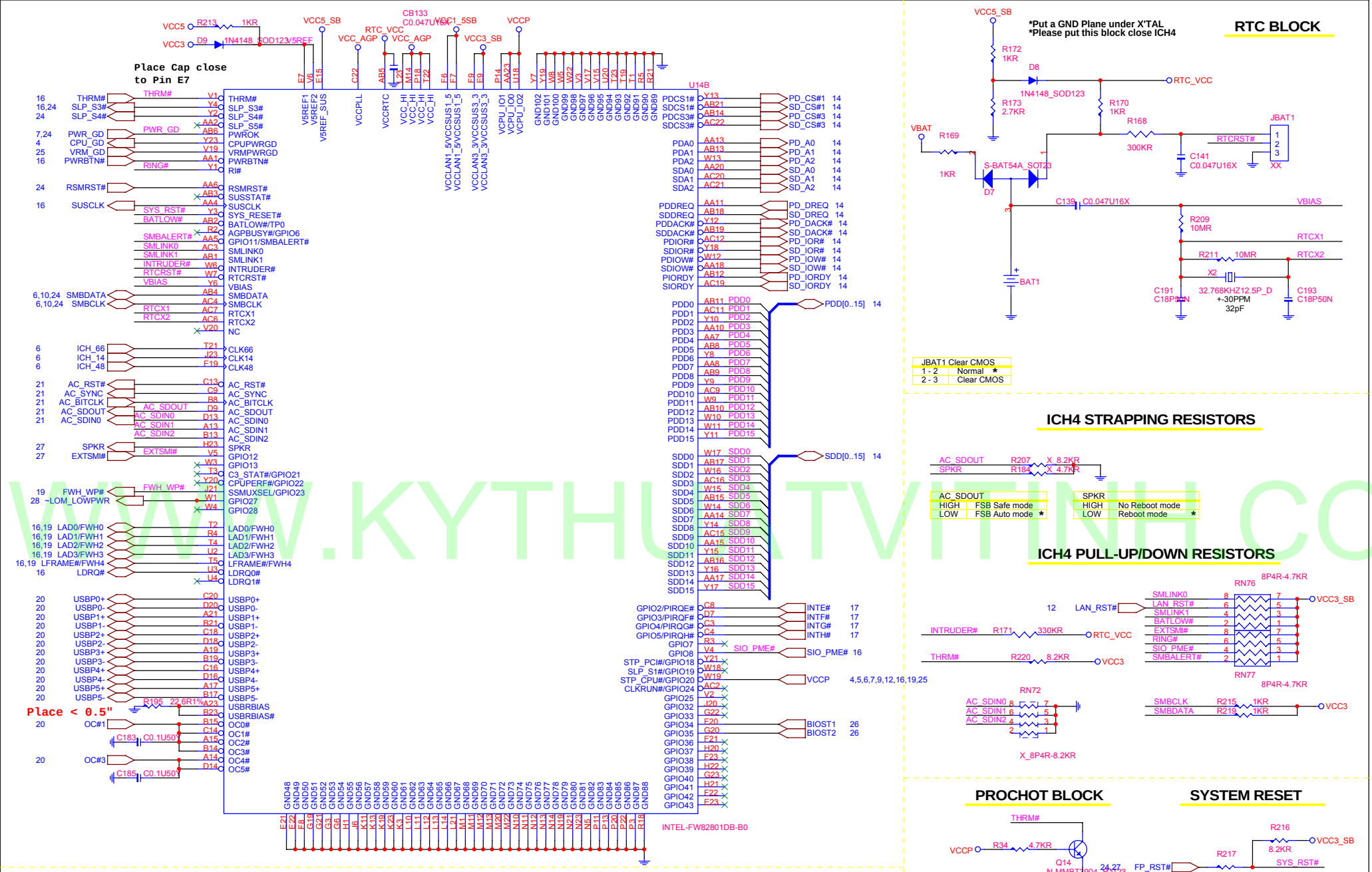

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Title	ICH4 ASIC/RTC/AC'97/GPIO/LPC/USB/IDE		
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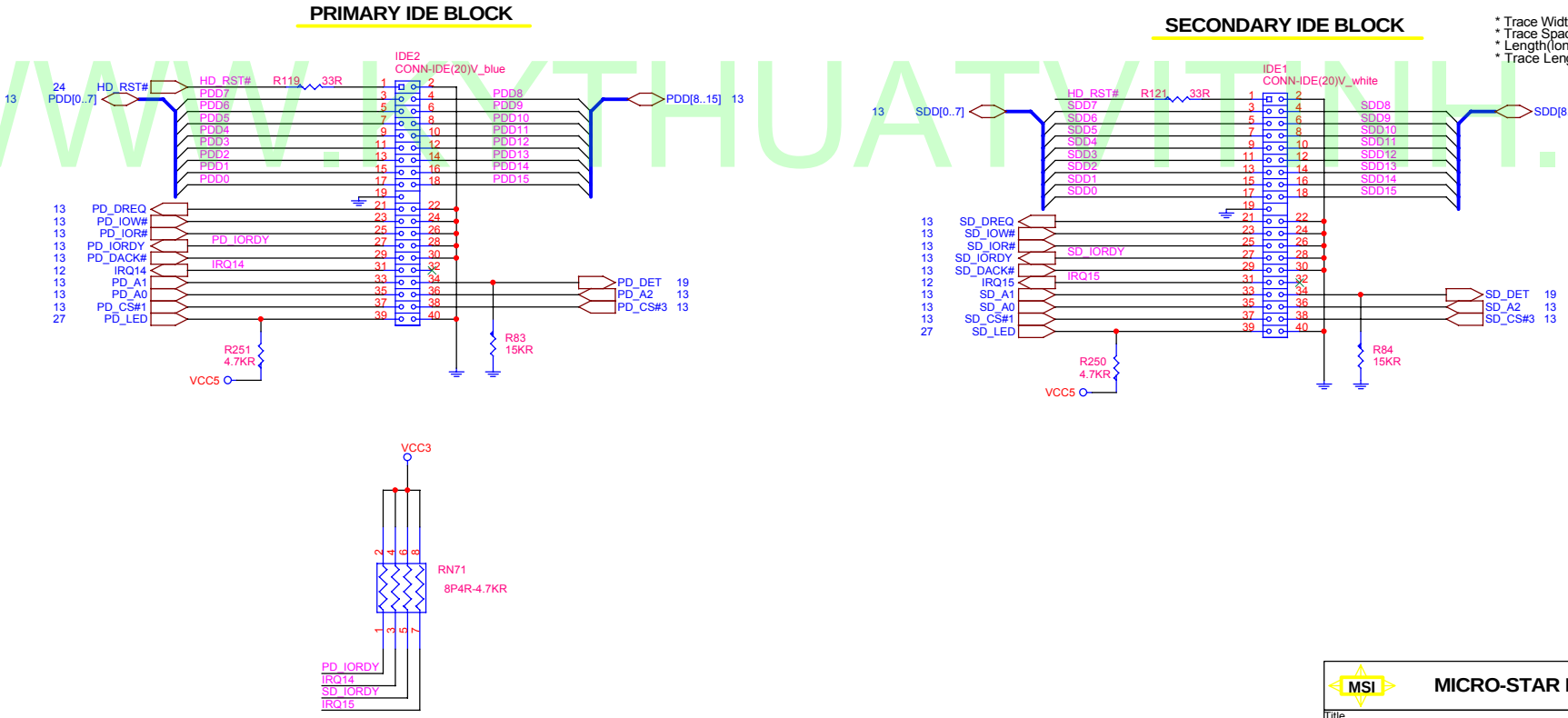
ATA100 IDE CONNECTORS



MSI	MICRO-STAR INT'L CO.,LTD.	
Title	ATA100 IDE Connectors 1&2	
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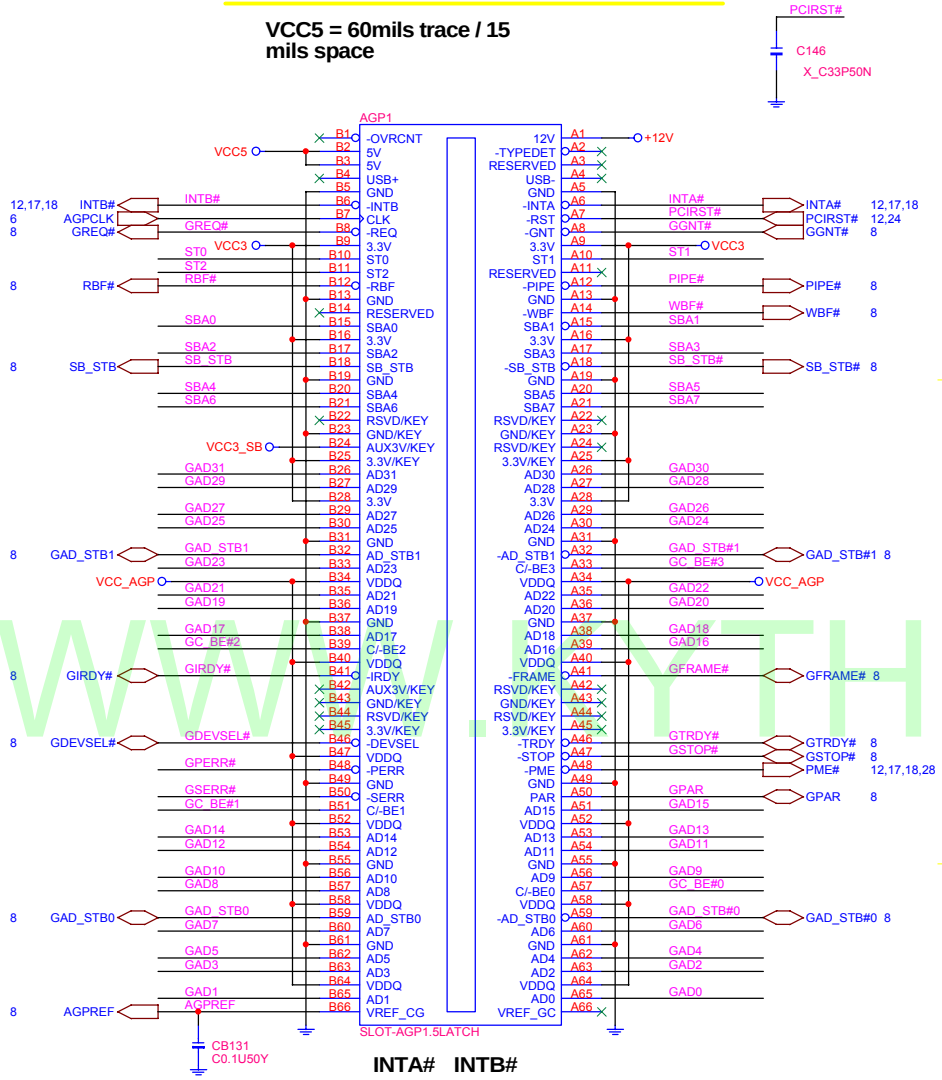
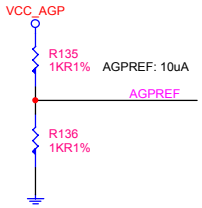
AGP 1.5V 2X/4X SLOT(AGP VER:2.0 COMPLY)

VCC5 = 60mils trace / 15 mils space

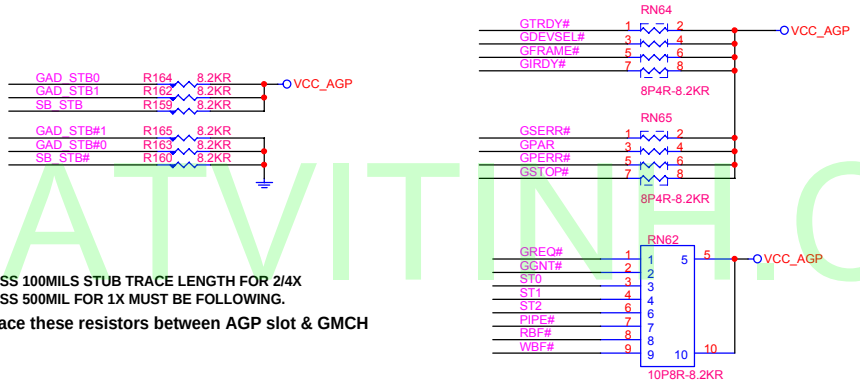


AGP SIGNAL REFERENCE CIRCUIT



NEAR AGP SLOT

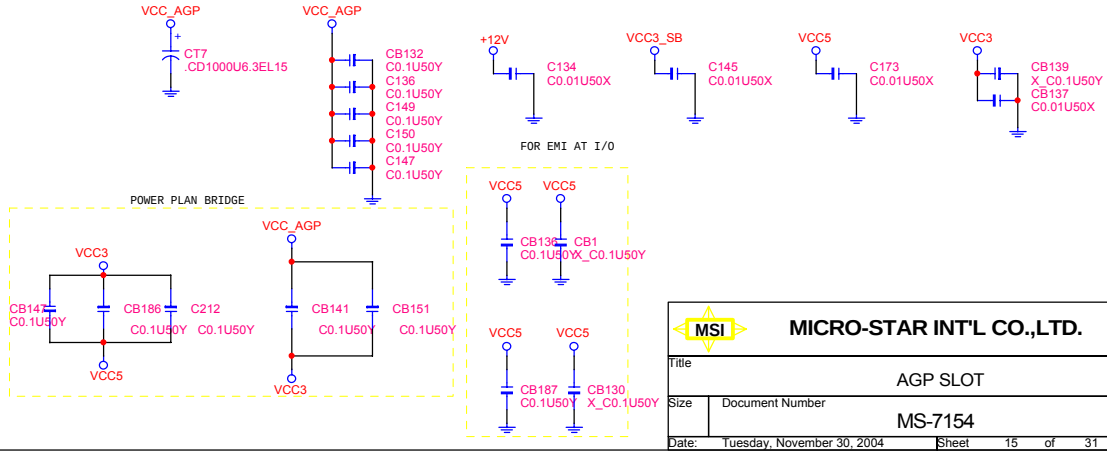
AGP TERMINATION RESISTORS



LESS 100MILS STUB TRACE LENGTH FOR 2/4X
LESS 500MIL FOR 1X MUST BE FOLLOWING.

Place these resistors between AGP slot & GMCH

AGP SLOT DECOUPLING CAPACITORS



ST[0..2] ST[0..2] 8
SBA[0..7] SBA[0..7] 8
GC_BE#[0..3] GC_BE#[0..3] 8
GAD[0..31] GAD[0..31] 8

MSI **MICRO-STAR INT'L CO.,LTD.**

Title	AGP SLOT	
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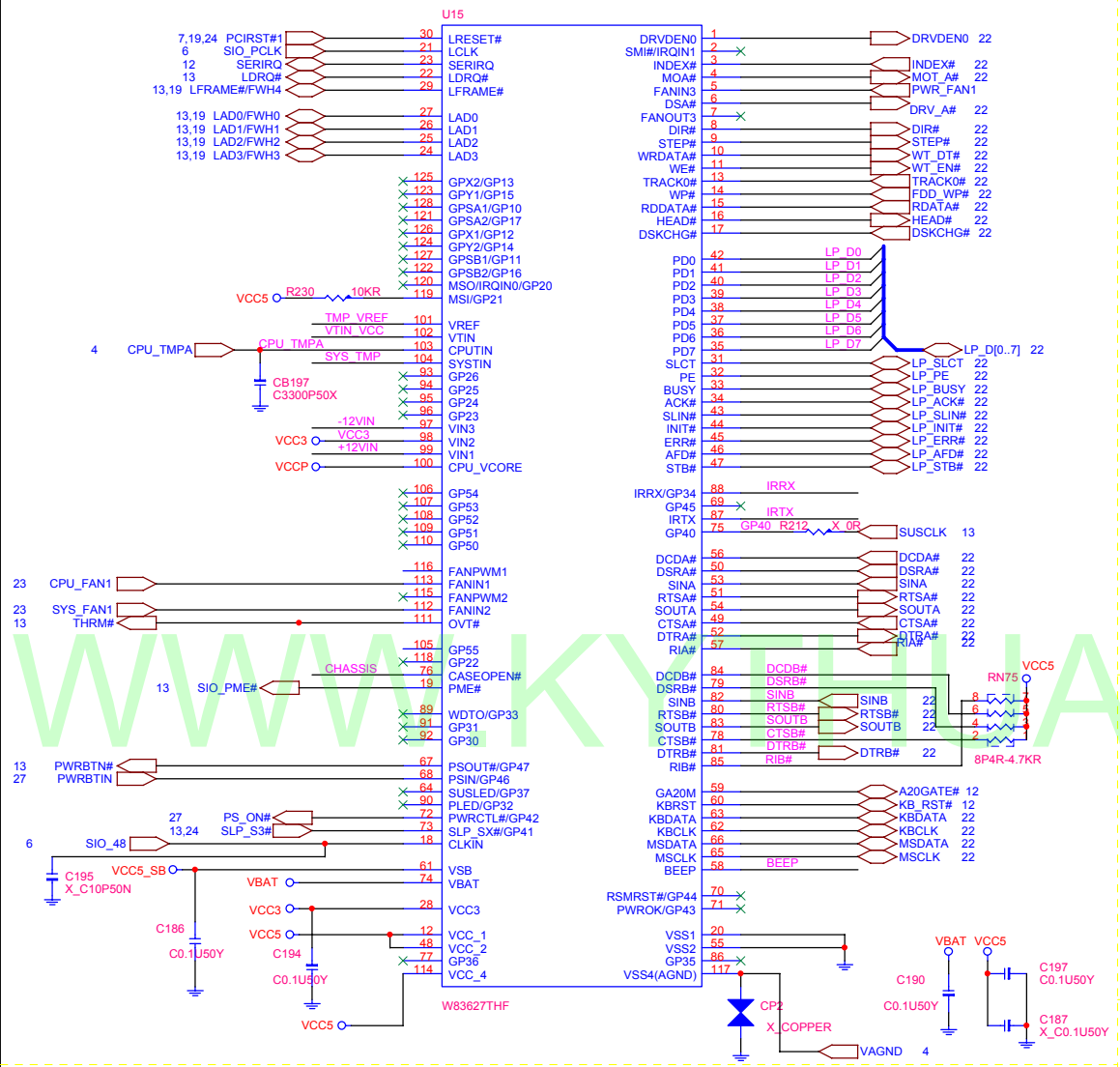
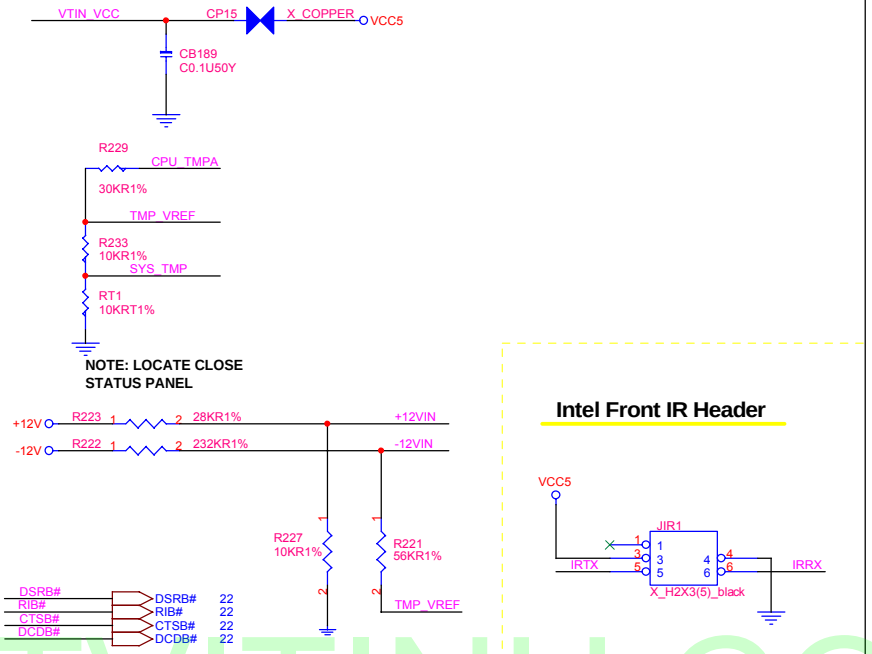
LPC SUPER I/O W83627HF/NHF/THF

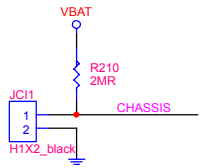


THERMAL RESISTOR BLOCK

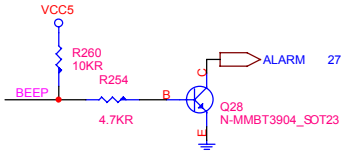


Intel Front IR Header

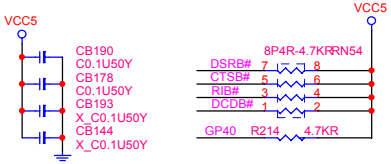
Chasis Intrusion Header



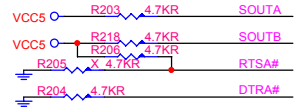
SPEAKER BLOCK



LPC I/O DECOUPLING CAPACITORS



LPC I/O STRAPPING RESISTOR



SOUTA	L: Disable KBC	H: Enable KBC
SOUTB	L: 24MHZ	H: 48MHZ
RTSA#	L: CFAD=2E	H: CFAD=4E
DTRA#	L: PNP Default	H: PNP no Default

MSI **MICRO-STAR INT'L CO.,LTD.**

Title	LPC IO & GAME PORT & DLED	
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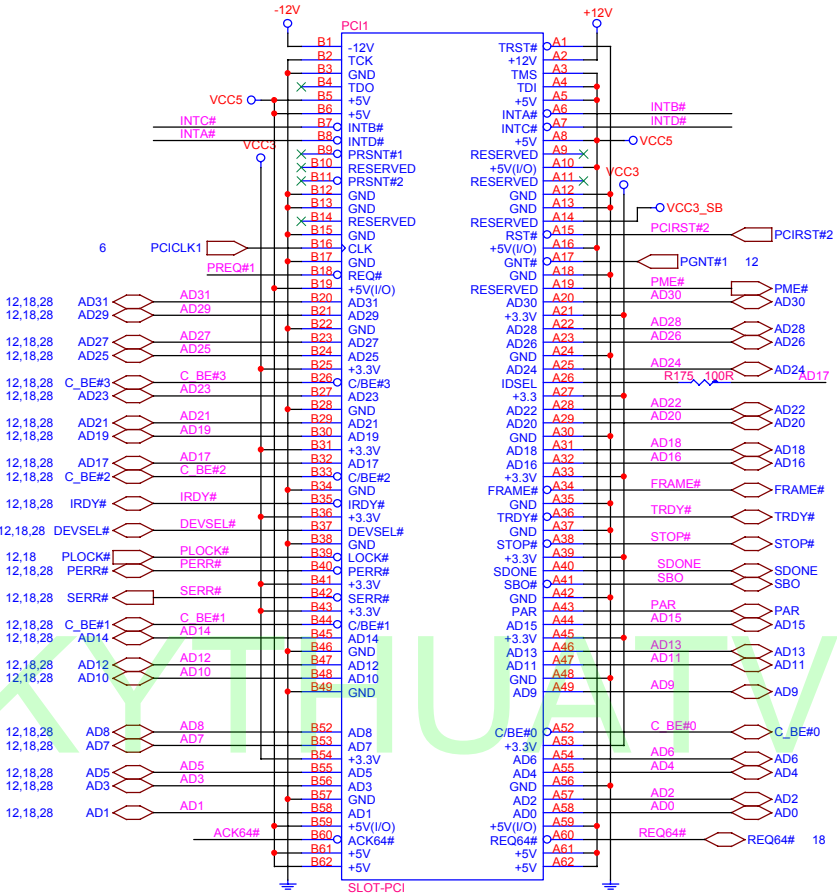
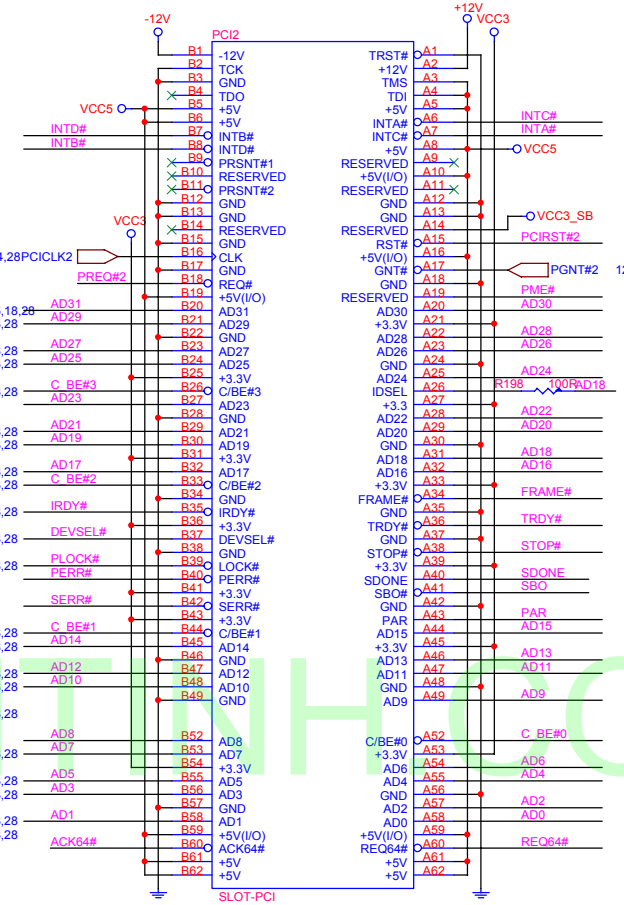
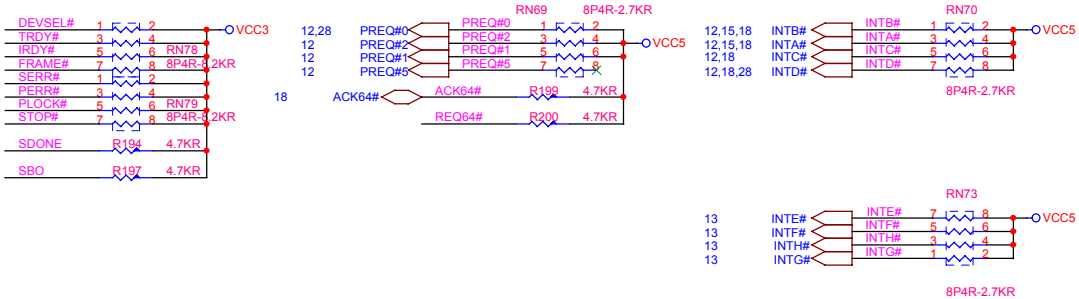
PCI SLOT 2 (PCI VER: 2.2 COMPLY)



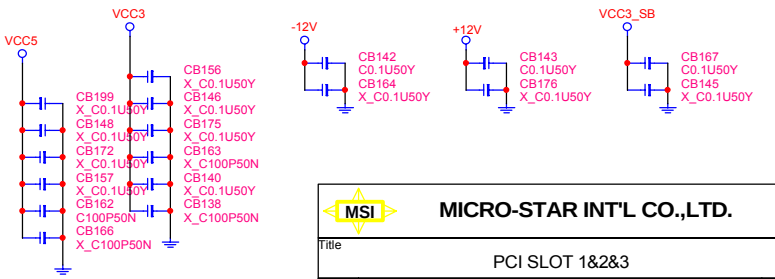
PCI SLOT 3 (PCI VER: 2.2 COMPLY)



PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



MICRO-STAR INT'L CO.,LTD.

Title	PCI SLOT 1&2&3	
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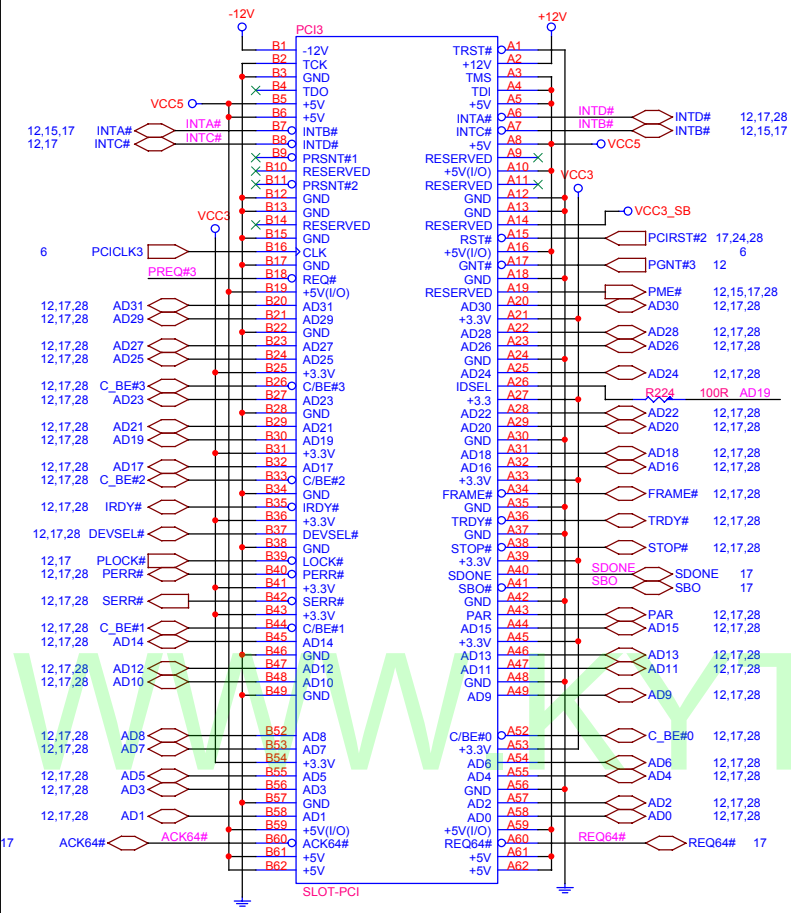
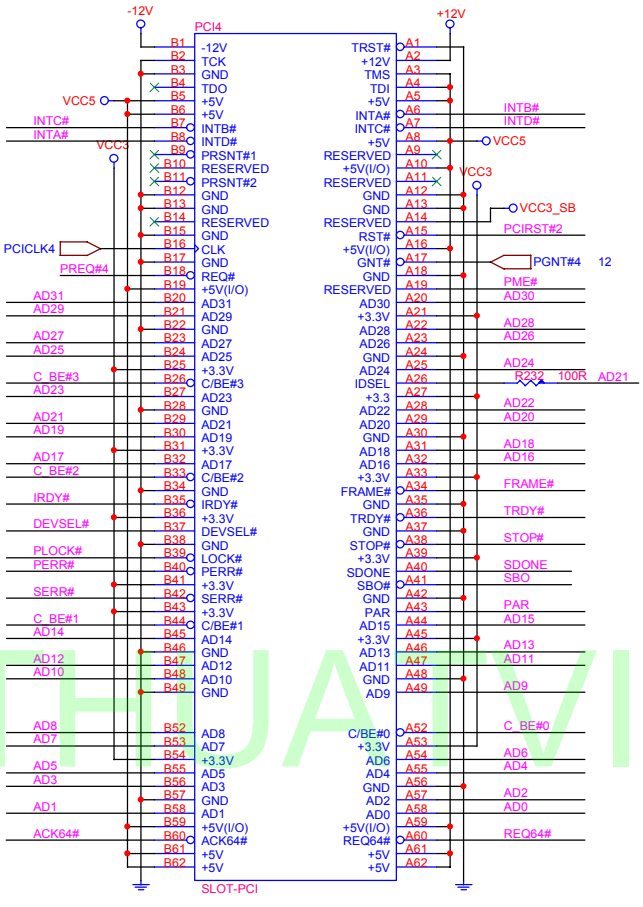
PCI SLOT 4 (PCI VER: 2.2 COMPLY)



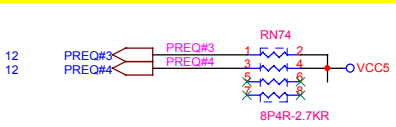
IDSEL = AD19
MASTER = PREQ3
INTD#

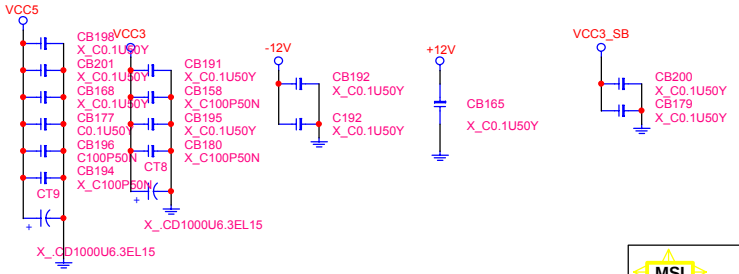
PCI SLOT 5 (PCI VER: 2.2 COMPLY)



IDSEL = AD21
MASTER = PREQ4
INTB#

PCI PULL-UP / DOWN RESISTORS





MSI MICRO-STAR INT'L CO.,LTD.

Title	PCI SLOT 4&5&6	
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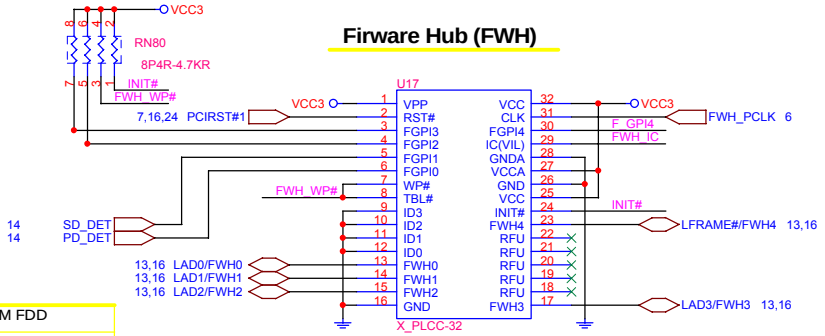
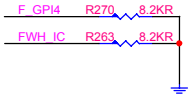
Firware Hub (FWH)



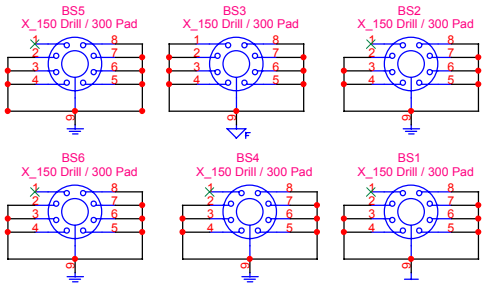
J6 Config.

1 - 2	FLUSH FROM FDD
2 - 3	BOOT AUTO CLEAR CMOS

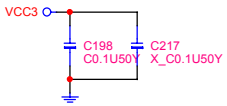
FWH RESISTORS



PCB Mounting Holes

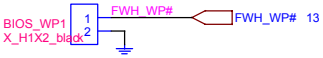


FWH DECOUPLING CAPACITORS



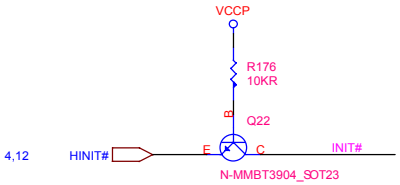
Place Cap. as Close to FWH< 350 mil

FWH write protect

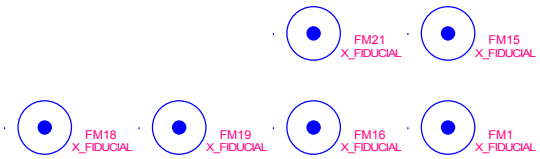


BIOS_WP	BIOS Update
SHORT	Locked
OPEN	Unlocked *

FWH INIT Signal Voltage Translation Block



PCB Fiducials



SIMULATION TRACE

MSI MICRO-STAR INT'L CO.,LTD.

Title	FWH	
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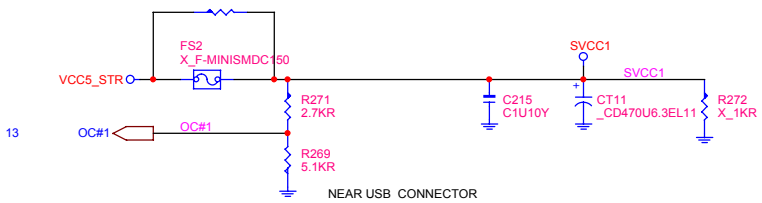
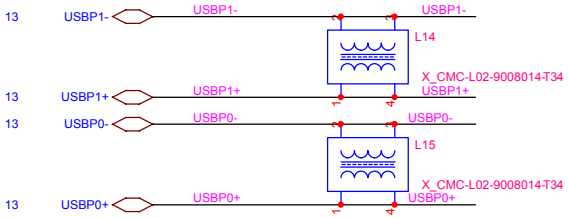
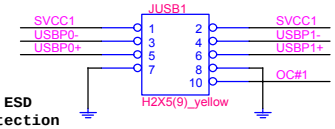
POWER CIRCUIT FOR USB PORT 0,1



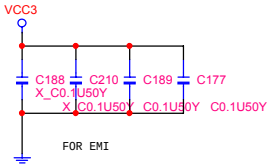
FRONT PANEL USB CONNECTOR FOR USB PORT 0,1

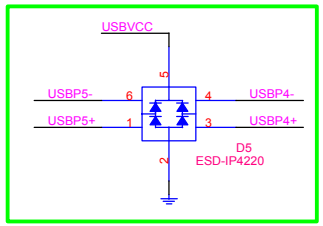


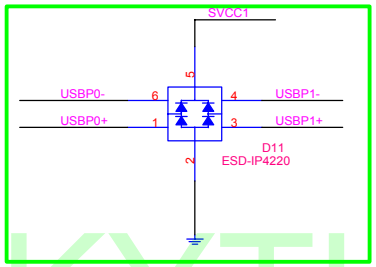
Intel Front USB Header



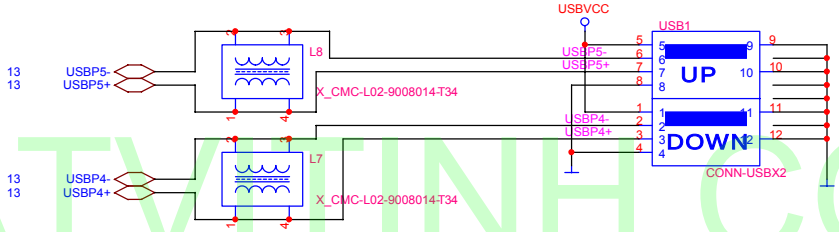
For ESD Protection



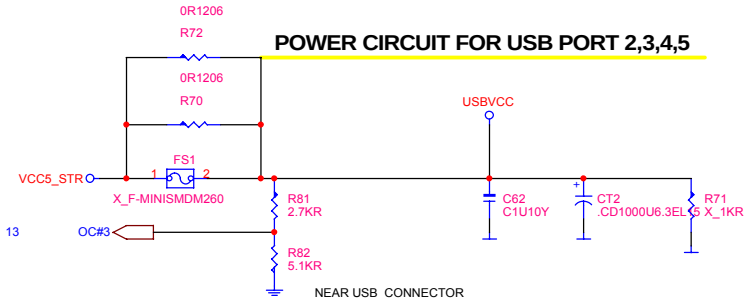


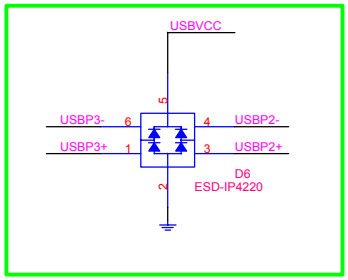


REAR PANEL USB CONNECTOR FOR USB PORT 2,3

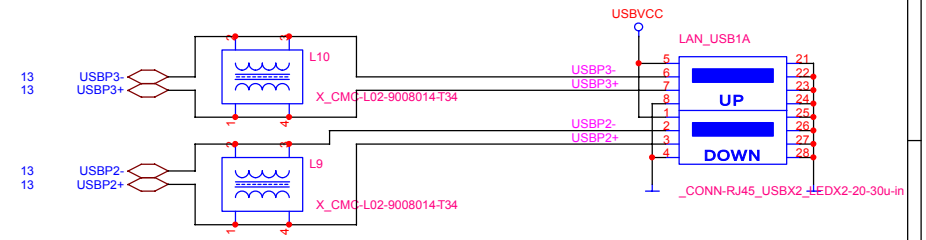


POWER CIRCUIT FOR USB PORT 2,3,4,5





REAR PANEL USB CONNECTOR FOR USB PORT 4,5



* USB Trace width : 9 mils
* USB Trace Spacing : 25 mils
* Differential USB Signlas Trace, Spacing : 18 mils
* USB Power Trace must be 40mils width

MSI MICRO-STAR INT'L CO.,LTD.

Title: USB CONNECTORS

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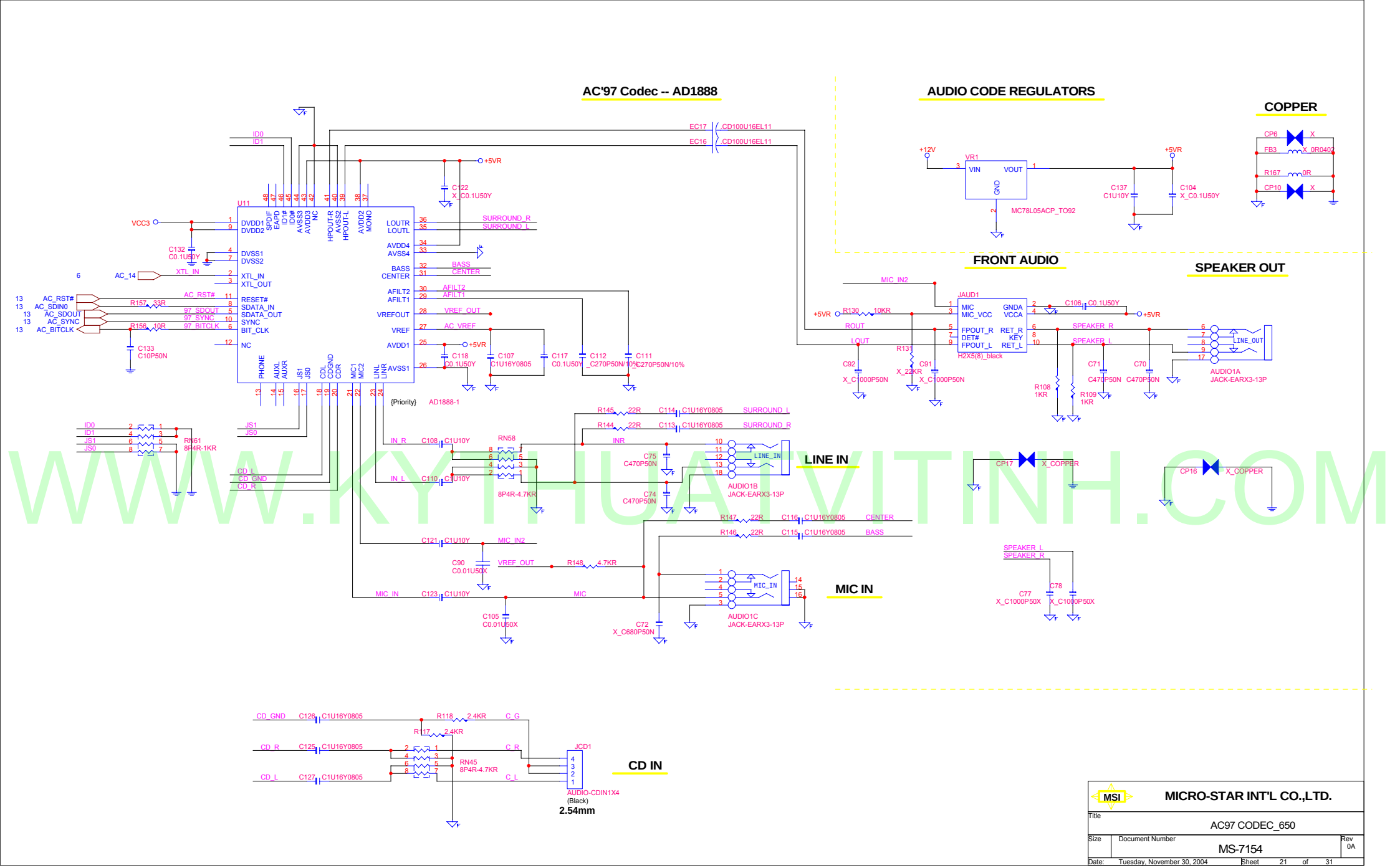
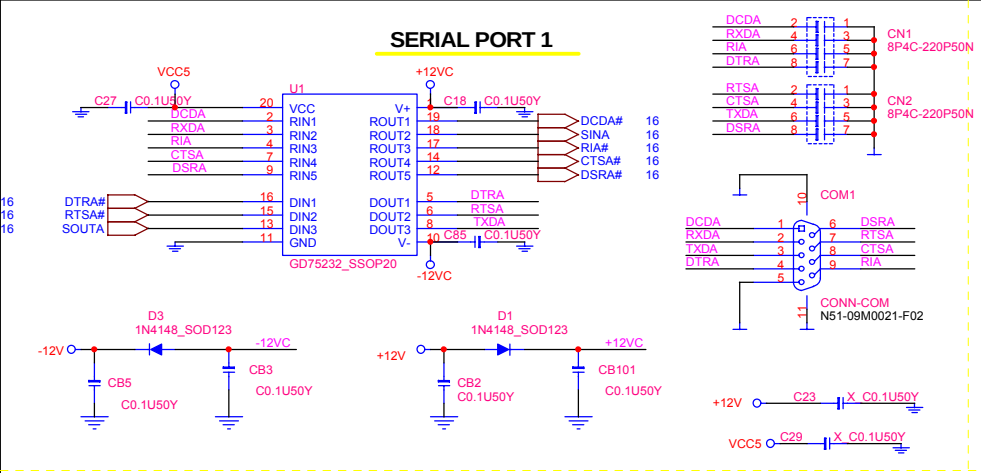
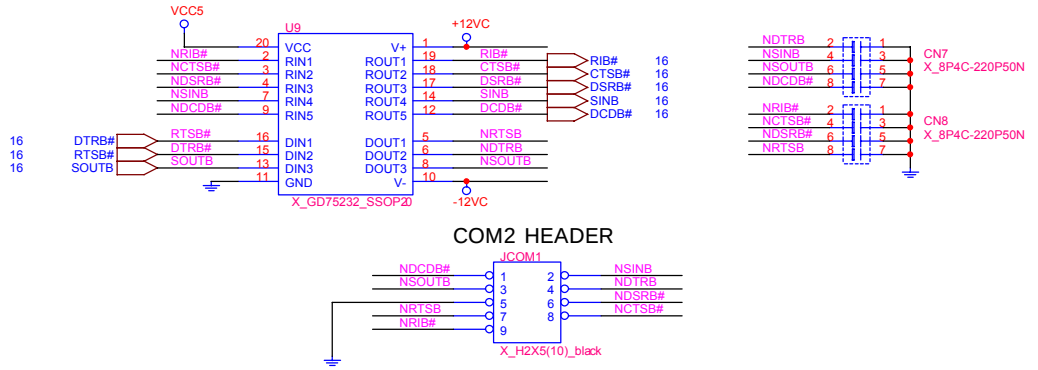


SERIAL PORT 1

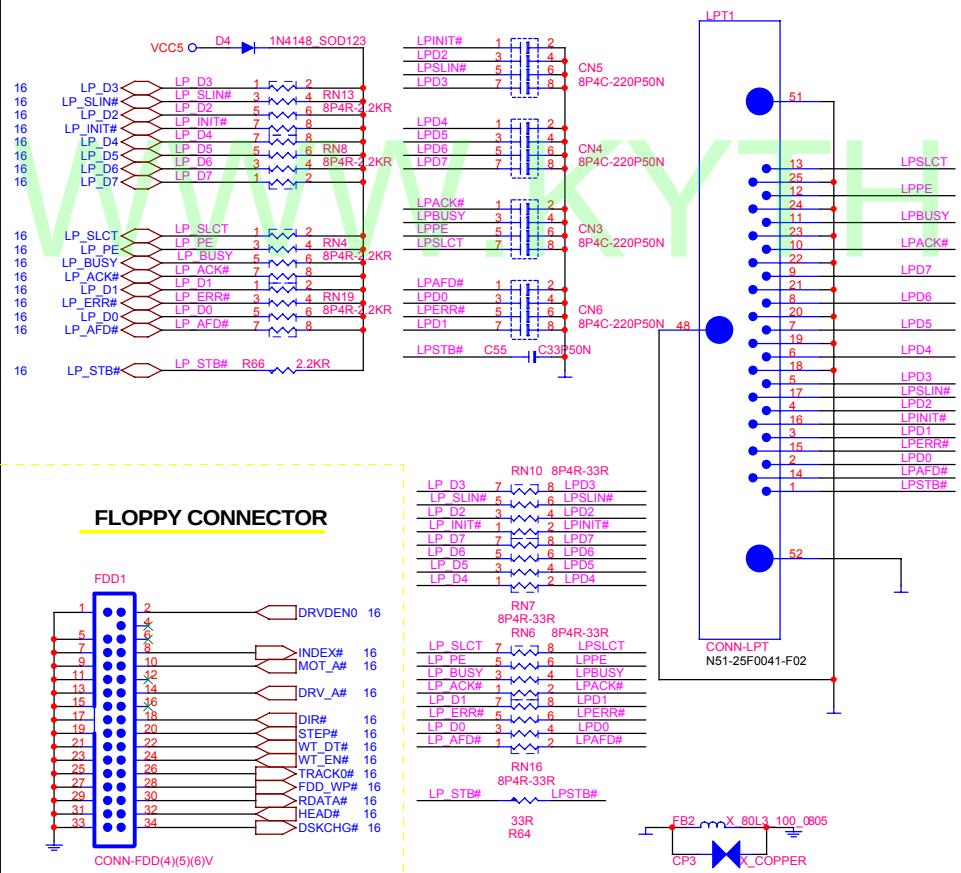


SERIAL PORT 2

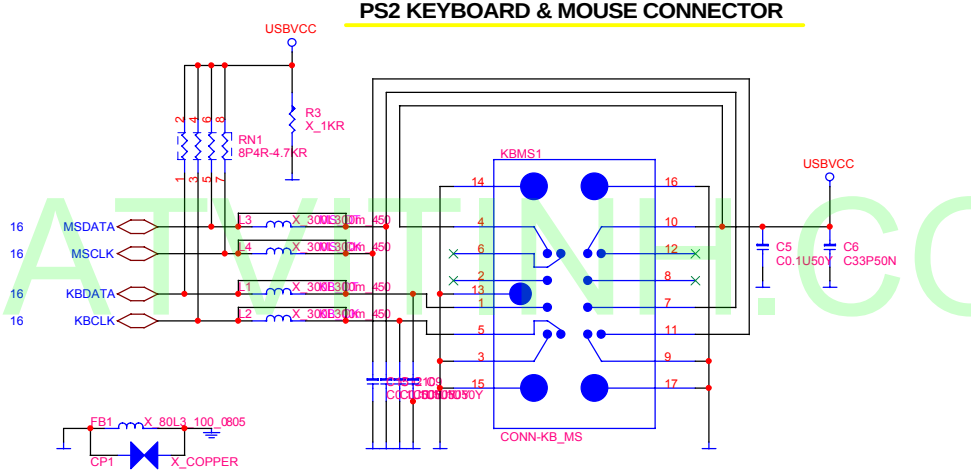


COM2 HEADER

PARALLAL PORT



PS2 KEYBOARD & MOUSE CONNECTOR



FLOPPY CONNECTOR

MSI MICRO-STAR INT'L CO.,LTD.

Title	I/O CONNECTORS	
Size	Document Number MS-7154	Rev 0A
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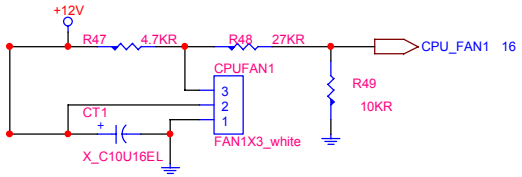
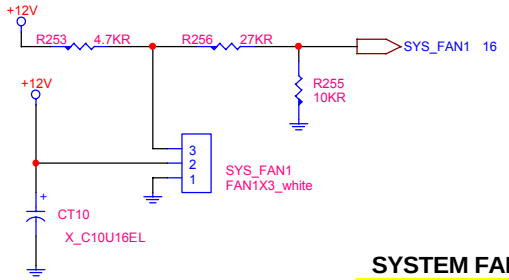
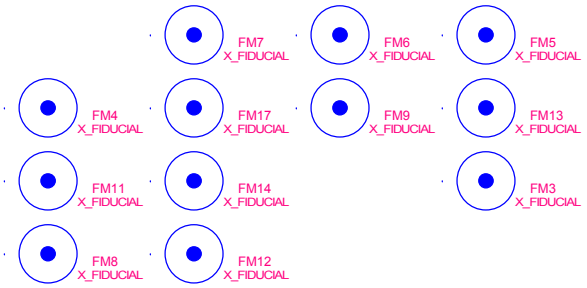


CPU FAN



SYSTEM FAN

COMPONENT Fiducials



MSI **MICRO-STAR INT'L CO.,LTD.**

Title	FAN Control	
Size	Document Number MS-7154	Rev 0A
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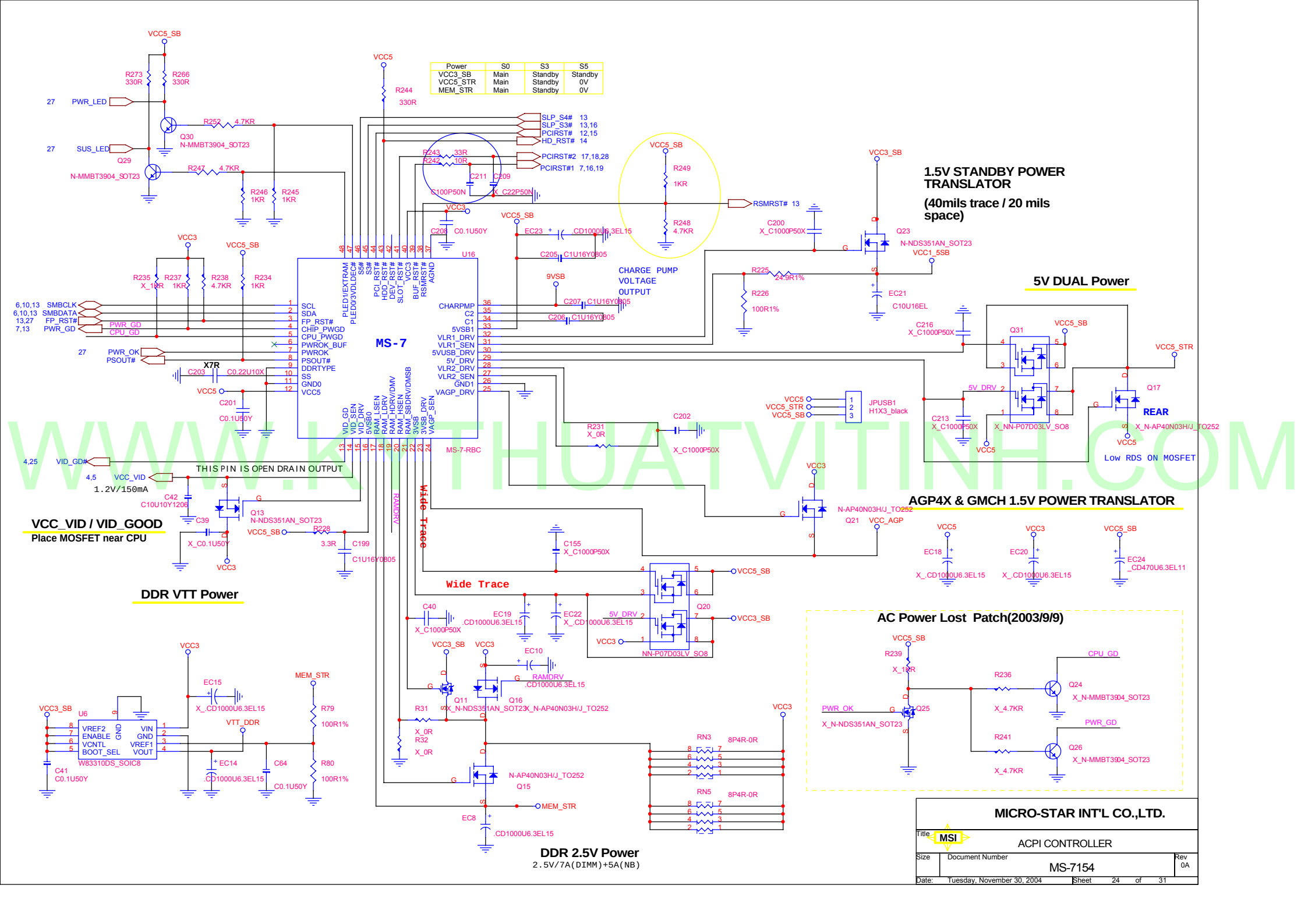

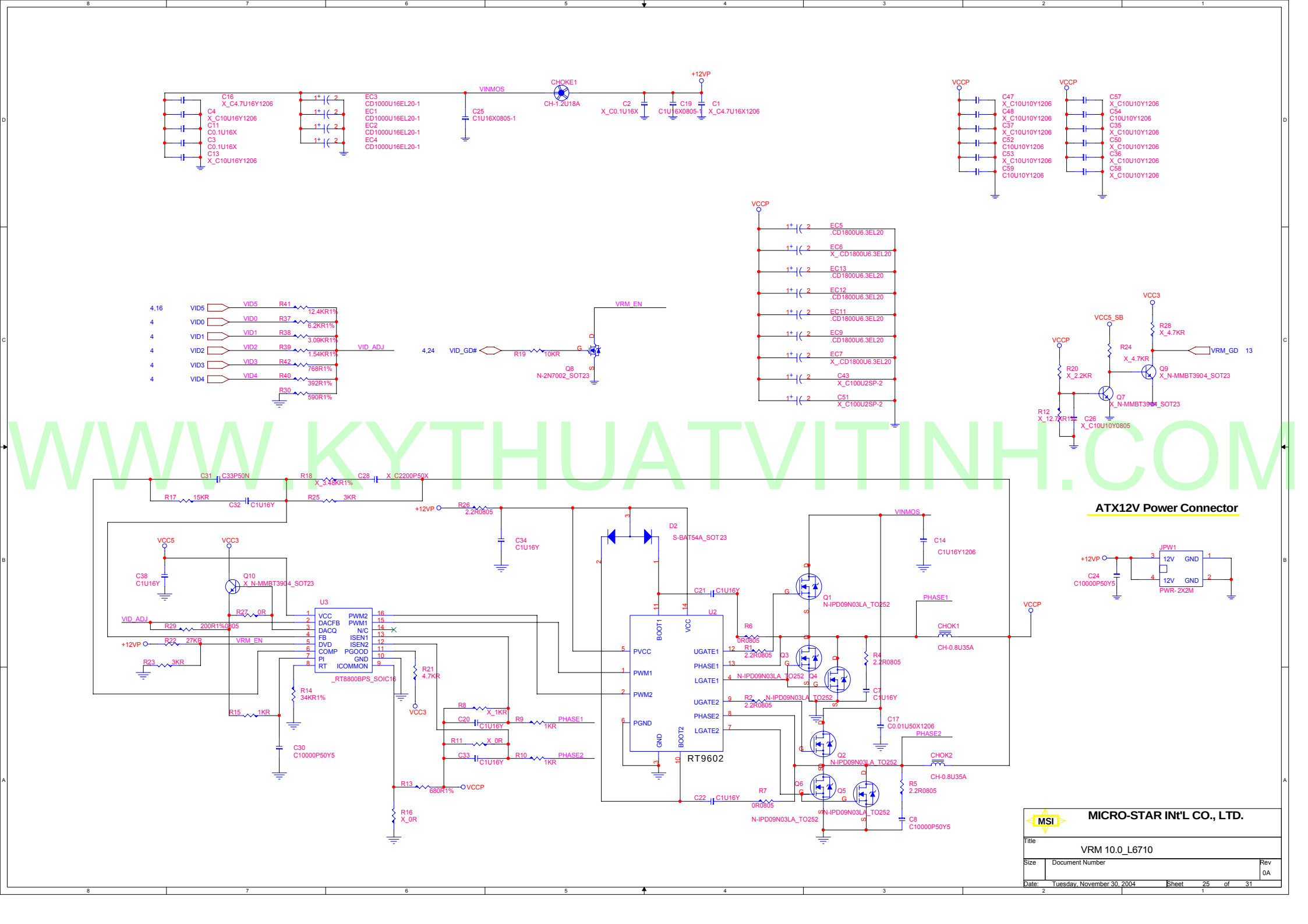

MSI MICRO-STAR INt'L CO., LTD.

Title: VRM 10.0_L6710

Size | Document Number | Rev 0A

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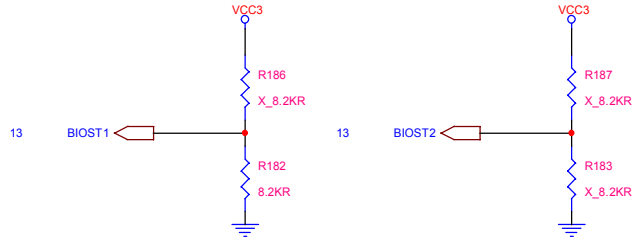
	BIOST1		
PE+LAN	0		STD
PE WITHOUT LAN	1		OPTION A



MICRO-STAR		
Title: DIAG LED		
Size: Custom	Document Number: MS-7154	Rev: 0A
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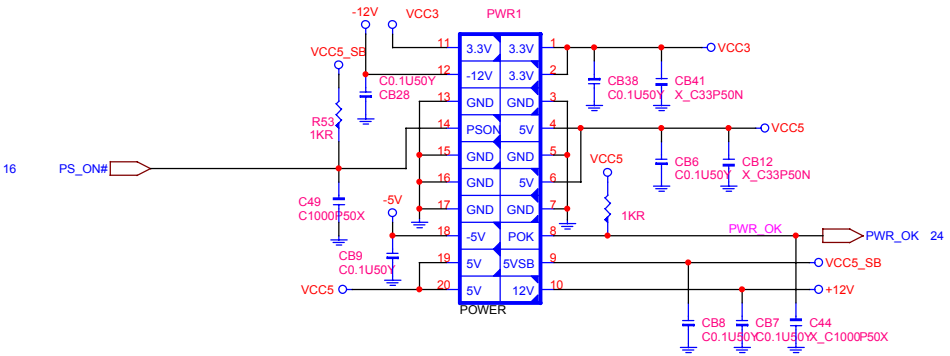
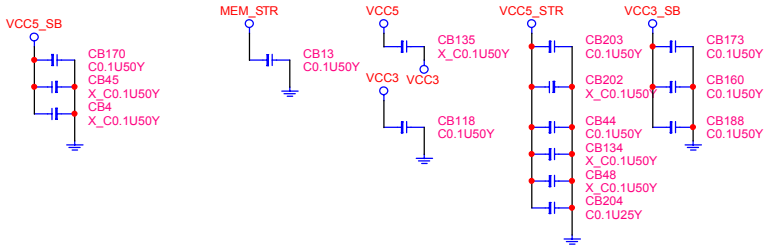
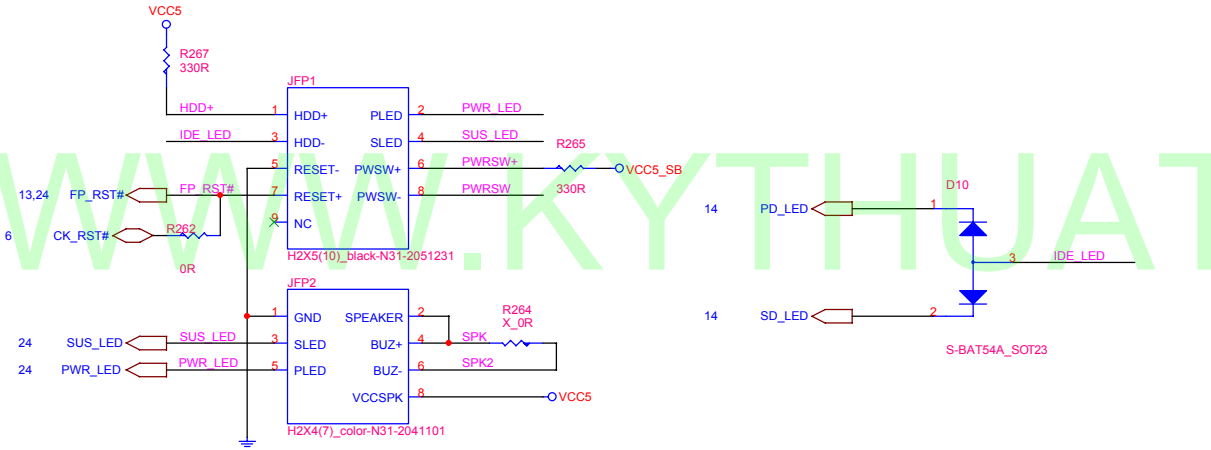
ATX CONNECTOR



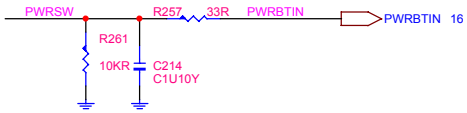
REGULATORS OUTPUT DECOUPLING CAPACITORS

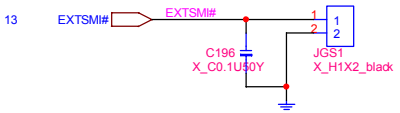


MSI/Intel Front Panel

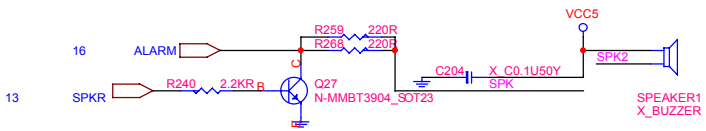


POWER BUTTON





SPEAKER



MSI MICRO-STAR INT'L CO.,LTD.

Title	Front Panel & ATX Connector & FAN	
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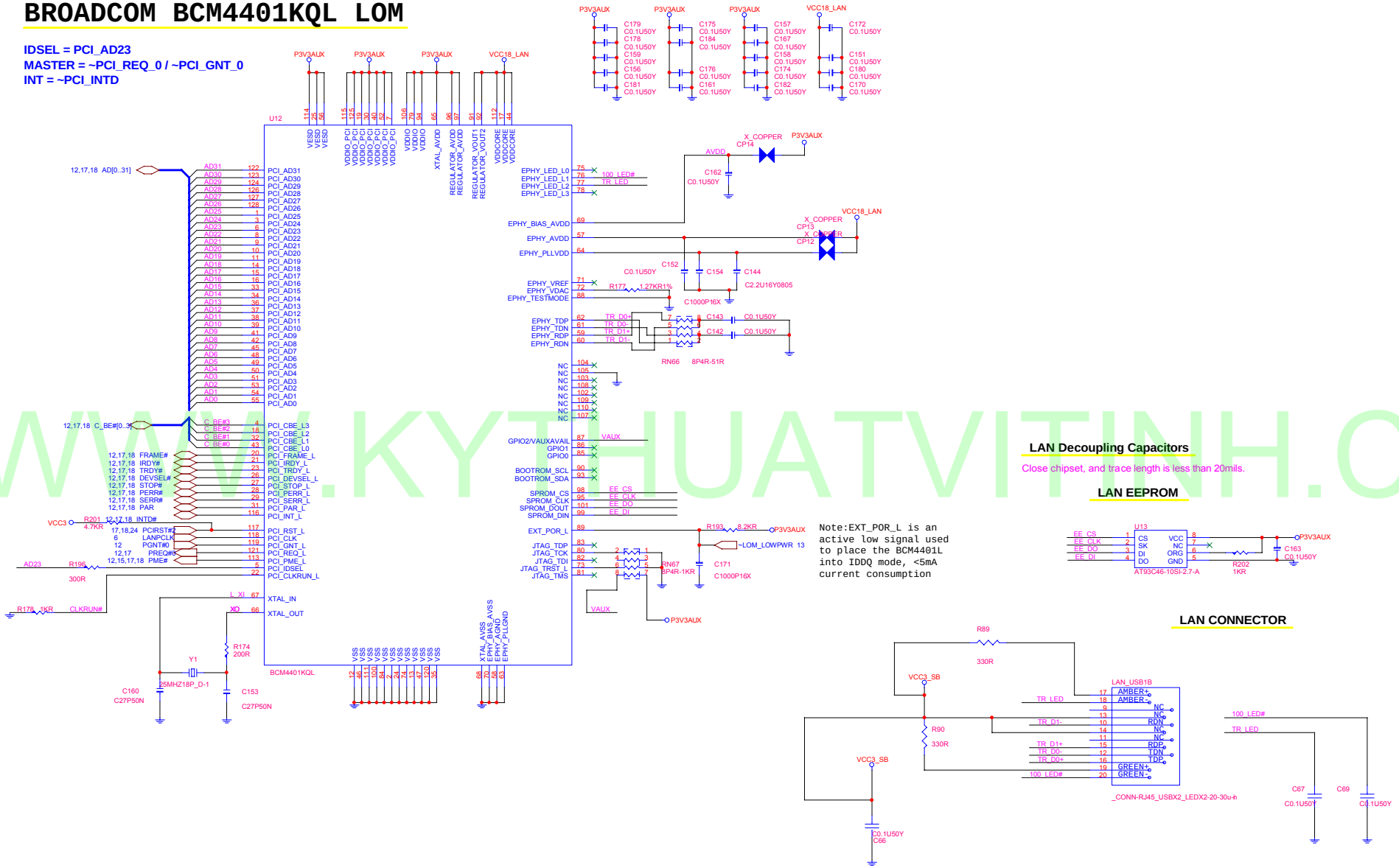
BROADCOM BCM4401KQL LOM

IDSEL = PCI_AD23
MASTER = ~PCI_REQ_0 / ~PCI_GNT_0
INT = ~PCI_INTD



Note:EXT_POR_L is an active low signal used to place the BCM4401L into IDDQ mode, <5mA current consumption

LAN Decoupling Capacitors

Close chipset, and trace length is less than 20mils.

LAN EEPROM

LAN CONNECTOR

MSI	MICRO-STAR INT'L CO.,LTD.	
Title	LAN RTL8101L	
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General SPEC

ICH4

GPIO Pin	Type	Function
GPIO 0	I	REQ#A (multifunction pin)
GPIO 1	I	PREQ#5 (multifunction pin)
GPIO 2	I	Pull up through 8.2K ohms (PIRQE#)
GPIO 3	I	Pull up through 8.2K ohms (PIRQF#)
GPIO 4	I	Pull up through 8.2K ohms (PIRQG#)
GPIO 5	I	Pull up through 8.2K ohms (PIRQH#)
GPIO 6	I	Pull down through 10K ohms (unused)
GPIO 7	I	Pull down through 10K ohms (unused)
GPIO 8	I	Pull Up to 3.3VSBY through 4.7K ohms (SIO_PME)
GPIO 9	I	Not Implemented
GPIO 10	I	Not Implemented
GPIO 11	I	SMB_ALERT (multifuntion pin)
GPIO 12	I	Pull down through 10K ohms (unused)
GPIO 13	I	Pull down through 10K ohms (unused)
GPIO 14~15	I	Not Implemented
GPIO 16	O	GNT#A (multifunction pin)
GPIO 17	O	PGNT#5 (multifuntion pin)
GPIO 18*	O	No Connected
GPIO 19	O	No Connected
GPIO 20	O	Vcore for cpu voltage adjusting
GPIO 21	O	No Connected
GPIO 22	OD	No Connected
GPIO 23	O	Pull Up to 3.3V through 8.2K ohms (BIOS protect)
GPIO 24	I/O	No Connected
GPIO 25	I/O	No Connected
GPIO 26	I/O	Not Implemented
GPIO 27	I/O	No Connected
GPIO 28	I/O	LAN DISABLE
GPIO 29~31	O	Not Implemented
GPIO 32	I/O	No Connected
GPIO 33	I/O	No Connected
GPIO 34	I/O	BIOST1 FOR BIOS SETTING
GPIO 35	I/O	No Connected
GPIO 36	I/O	No Connected
GPIO 37	I/O	No Connected
GPIO 38	I/O	No Connected
GPIO 39	I/O	No Connected
GPIO 40	I/O	No Connected
GPIO 41	I/O	No Connected
GPIO 42	I/O	No Connected
GPIO 43	I/O	No Connected
GPIO 44~47	I/O	Not Implemented

** GPIO18 will toggle at 1Hz frequency.*

FWH

GPIO Pin	Type	Function
GPI 0	I	ATA IDE1 DETECT
GPI 1	I	ATA IDE2 DETECT
GPI 2	I	P1 customer defined
GPI 3	I	P1 customer defined
GPI 4	I	Pull down through 8.2K ohms (unused)

PCI Config.

DEVICE	ICH INT Pin	IDSEL	CLOCK	CLK GEN PIN OUT
PCI Slot 1	INTB# INTC# INTD# INTA#	AD17	PCICLK1 PREQ#1 PGNT#1	15 (PCI3)
PCI Slot 2	INTC# INTD# INTA# INTB#	AD18	PCICLK2 PREQ#2 PGNT#2	16 (PCI4)
PCI Slot 3	INTD# INTA# INTB# INTC#	AD19	PCICLK3 PREQ#3 PGNT#3	14 (PCI4)
PCI Slot 4	INTB# INTC# INTD# INTA#	AD21	PCICLK4 PREQ#4 PGNT#4	13 (PCI1)
PCI Slot 5	INTA# INTB# INTC# INTD#	AD20 AD16	PCICLK5 PREQ#5 PGNT#5 PREQ#1 PGNT#1	19 (PCI5) 12 (PCI0)
LAN	INTE# INTF#	AD29	LANPCLK PREQ#0 PGNT#0	20 (PCI6)

**ICH4 reserved PCI address line AD22 for the PCI-to-ISA Bridge's IDSEL input.*

Note 1:PCI Slot 1and 6(2nd Device) are share with PREQ#1,PGNT#1.

DLED-Super I/O

GPIO Pin	Type	Function
GPBX/GP13	I/OD	LED#4
GPAY/GP15	I/OD	LED#2
GPAS1/GP10	I/OD	LED1
GPAS2/GP17	I/OD	LED4
GPAX/GP12	I/OD	LED#3
GPBY/GP14	I/OD	LED#1
GPBS1/GP11	I/OD	LED2
GPBS2/GP16	I/OD	LED3

DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	1010000B	DCLK0/DCLK0# DCLK1/DCLK1# DCLK2/DCLK2#
DIMM 2	1010001B	DCLK3/DCLK3# DCLK4/DCLK4# DCLK5/DCLK5#

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Title: General SPEC

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2 P-22 TO REMOVE COM2

Revision Initial ver: 0A on 2/06/02

1.2/22/02 PM CHANGE SPEC FOR LAN FROM REALTECH TO INTEL

Revision Initial ver: 10 on 3/28/02

1.CHANGE THE NB FOOTPRINT FROM 820 PIN TO 760 PIN
2.TO MODIFY THE SCOURCE VOLTAGE OF VTT_TERM FROM VCC3_SB TO MEM_STR
3.CHANGE CODEC FROM ALC201 TO ALC202A

Revision Initial ver: 10A on 4/03/02

1.TO MODIFY THE DIMM2,3 CLOCK TOPOLOGY
2.EMI ISSUE FOR LAN
3.R395,R396 AT 0 OHM FOR LAN'S TX PAIR EMI ISSUE.
4.C164 ADD 10p TO GND FOR AC_BCLK'S EMI ISSUE
5.C213,C214,C215 ADD 104p AT VGA PART FOTR EMI ISSUE
6.C219,C220 ADD 104p AT USB2 PART FOR EMI ISSUE
7.CB176,CB256 ADD 104p AT 1/O FOR EMI ISSUE.
8.CN12,CN13 ADD 10p AT PCICLKS FOR EMI ISSUE
9.R377~R388 ADD 0 OHM AT SOLDER SIDE FOR DIMM2,DIMM3 CLOCK
10.C151,C152,C156,C163,MDM_IN1,AUX_IN1 REMOVED FOR COST-DOWN
11.TO REMOVE FLASHROM HOLDER AND FLASHROM CHANGED 50 5010 LEVEL FOR COST-DOWN.
12.JVGA1 CONNECTOR'S PARTNUMBER WAS ERROR AND CHANGED IT.
13.R244 CHANGE FROM 15 OHMS TO 22.6 OHMS FOR USB VBIAS FROM INTEL RECOMMEND.

Revision Initial ver: 20 on 5/23/02

1.To change spec about dimm,3dimms changed to 2dimms
2. Co-layout the VGA connector and com port because for next generatation nb of intel(845PE without vga signals)
3.To modify the dimension of PCB(30.5cmX20.5cm)
4.The pcirst# of agpslot chang from pcirst#2 to pcirst#(p-15)
5.To remove ioslation circuity of smbus.
6.To add a cap of 1000u/6.3V for VCC3 translate to VCC3_SB(P-26)
7.To add a circuity for rsmrst# when plug out the atx power that can quickly cut off the signal(P-26)
8.To remove sktocc# from cpu to clock ren.(P-6)
9.Rename JCASE1 -> JCI1,IR1->jIR1,JAUDIO1->JAUD1.

Revision Initial ver: 20A on7/1/02

1.(P-13) To add "slp_s4#" trace to MS-5 to fix the issue of vdimm that can not be close at S4.
2.(P-18,19) To add a damping resistoes at the IDSEL of PCIs .
3.(P-22) To change audio from 2 channels to 6 channels and add a mic2 thrae to rear side for central output.
4.(P-27) To support FMB2 spec and add a mosfet of low side for each phase.
5.(P-29) To move the JBT1 connector from pci5 to jusb2 for signal qulity.
6.(P-13) To modify the battry power of SI/O from BAT1 directly..

Revision Initial ver: 300 on 6/02/03

1 P-30 TO CHANGE LAN'S SPEC FROM INTEL PHY(82562ET) TO PCI LAN (RTL8101L).
2 P-24 TO REMOVE COM2
3 P-21 MODIFY I/O SHEILD LOCATION JUSB2 MOVE TO REARE SIDE AND REMOVE GAME PORT

Revision Initial ver: 500 on 7/15/03

1 P-30 TO CHANGE LAN'S SPEC FROM PCI LAN (RTL8101L) TO PCI LAN (RTL8100C).
2 P-6 TO CHANGE Clock Gen. FROM ICS950335CF TO ICS952611AF.
3 P-25 TO CHANGE CPU Power SPEC from VRM 9/0 to VRM 10/0.
4 P-21 TO CHANGE AC97 CODEC from ALC650 to ALC655.
5 P-24 TO CHANGE ACPI Controler from W83302D(MS6) to MS7.
6 P-18 Removed PCI SLOT1.
7 P-17 TO CHANGE SIO from W83627HF-AW to W83627THF.
8 P-23 CPU FAN Support SMART FAN Function.
9 P-20 MODIFY I/O SHEILD LOCATION USB1 to RCA_USB(with SPDIF Output) near LAN_USB.

Revision Initial ver: 50A on 9/22/03

1 P-21 Add FR_MIC Ref_voltage to +5VR.
2 P-6 FS-0 Strping to "0".
3 P-21 Add 1uF Cap(C11). to Vef of AC97 CODEC.
4 P-11 TO CHANGE 0.1uF to 1uF of VTT_DDR Power.

Revision Initial ver: 50B on 10/28/03

1 P-18 Changed PCI5 SPEC
Add 2 PCI MASTER
Add Audio Signal
Add USB VCC
Add Smbus Signal

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